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CONDUCTION THROUGH THIN FILMS OF SEMICONDUCTORS

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A THESIS SUBMITTED

TO

THE UNIVERSITY OF POONA

FOR

THE DEGREE OF DOCTOR OF PHILOSOPHY
(IN CHEMISTRY)

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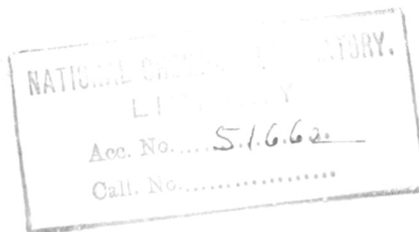

by

SHASHIKUMAR GUNDA PATIL, M.Sc.,
NATIONAL CHEMICAL LABORATORY, POONA.

MARCH, 1967.

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(S. G. Patil)

National Chemical Laboratory,
Poona-8.

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List of symbols

No.	Description	Symbol
1.	Thickness of the insulating film	L
2.	Effective area of cross-section of the sample	S
3.	Current	I
4.	Current density (I/S)	J
5.	Applied voltage across the sample	V
6.	Electric field across the sample	F
7.	Boltzman constant	k
8.	Dielectric constant	ϵ
9.	Band gap	ΔE
10.	Total electronically affective defect states	N_{def}
11.	Total electron trap density	N_t
12.	Charge and mass of electrons and holes respectively.	e_n, m_n e_p, m_p
13.	Mobility of electrons and holes respectively	μ_n, μ_p
14.	Common life time for carriers	τ
15.	Life time for electrons and holes respectively	τ_n, τ_p
16.	Transit time for electrons and holes respectively	t_n, t_p
17.	Capture cross-section for electrons and holes respectively	σ_n, σ_p
18.	Free carrier densities of electrons and holes respectively in thermal equilibrium with traps	n_o, p_o
19.	Injected carrier density of electrons and holes respectively	n, p
20.	The ratio of the free to trapped electron densities	θ

GENERAL INTRODUCTION

GENERAL INTRODUCTION

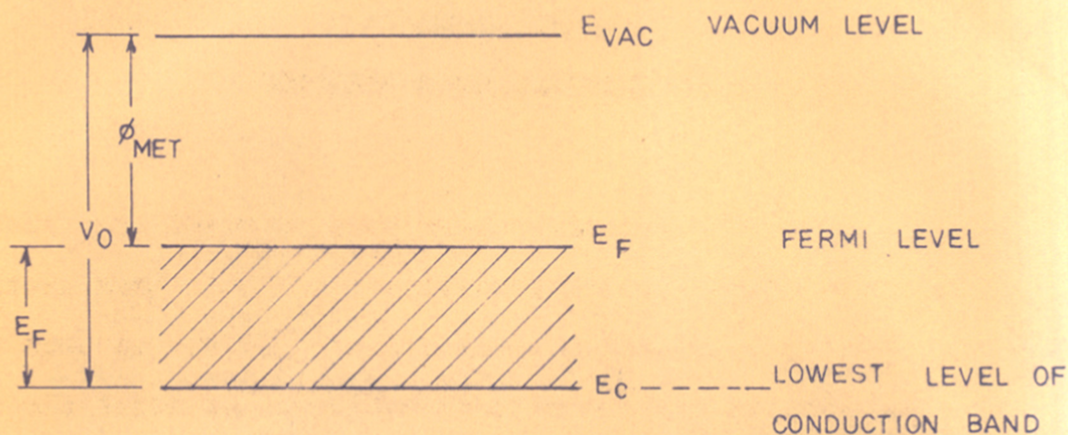
When a voltage is applied across a thin film (say 100Å thick) of an insulator, in general, one gets current densities much higher than what one would expect from the bulk specific resistivity values. Several mechanisms have been proposed for the electronic conduction through these thin films of insulators. The exact mechanism of conduction depends upon the nature of the metal and the insulator, the thickness of the insulating film, the ambient temperature, the electrical field, etc. The importance of the study of electronic conduction through these films has increased during recent years, in view of their possible applications in several electronic devices such as thin film tunnel diodes, thin film transistors, negative resistance devices, Gunn diodes, etc. Thin film studies are also important for investigations in the field of superconductors, lasers, electroluminescent materials, etc.

Recent studies have revealed that cadmium sulphide films can find applications in field-effect transistors, negative resistance devices and in microcircuits. During the course of our studies on the diode structures prepared by sandwiching cadmium sulphide film between two aluminium electrodes, we have observed a new phenomenon of dual negative resistance. In the following chapters we present a detailed account of the phenomenon.

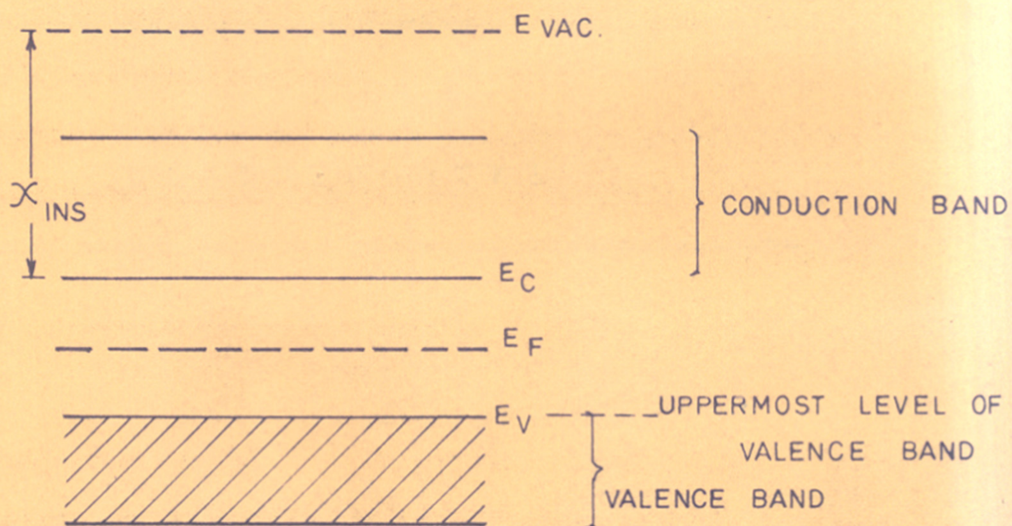
The first chapter summarises the different mechanisms suggested by the earlier workers to explain the high current density and the negative resistance observed in the current-voltage characteristics of such structures. In the second chapter we describe the experimental techniques used for the preparation and study of the sandwich structures. In the third chapter the experimental results are described. The discussion of the results and the proposed model for the dual negative resistance is given in the last chapter.

CHAPTER - I

INTRODUCTION



a)



b)

FIG.1. SCHEMATIC ENERGY-BAND DIAGRAM FOR

a) METAL

b) INSULATOR

CHAPTER - I

A) MECHANISMS OF CONDUCTION

Various mechanisms have been proposed to explain the current-voltage characteristics of thin insulator films, sandwiched between two metal films. Before we come to these mechanisms it will be better to discuss in brief the well-known properties of metal-insulator junctions.

The electrons responsible for conduction in metals occupy a partially filled conduction band [Fig. 1(a)]. The total number of conduction electrons are distributed over the available energy states according to the Fermi-Dirac statistics. The probability that a state 'E' is occupied by the electron is given by[1]

$$P(E) = \frac{1}{1 + \exp\left(\frac{E-E_F}{kT}\right)} \qquad \ldots(1)$$

where E_F is the Fermi level. It can be seen that the Fermi energy is the energy level at which the electron density distribution function has a value equal to half. At $T = 0^\circ K$ all levels upto the Fermi level are occupied by electrons and all levels beyond are empty. V_o is the depth of the bottom of the conduction band from the vacuum level which is the potential energy of the electron out side the metal. $\phi_{met} = V_o - E_F$, is

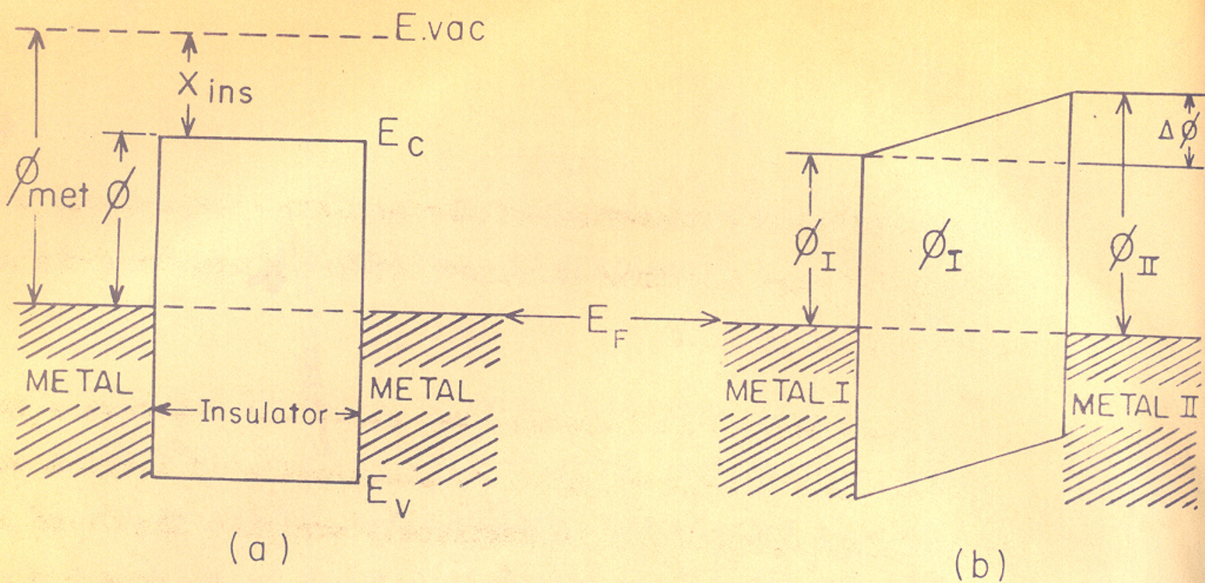


Fig.2 SCHEMATIC ENERGY BAND DIAGRAM FOR METAL-INSULATOR-METAL DIODE

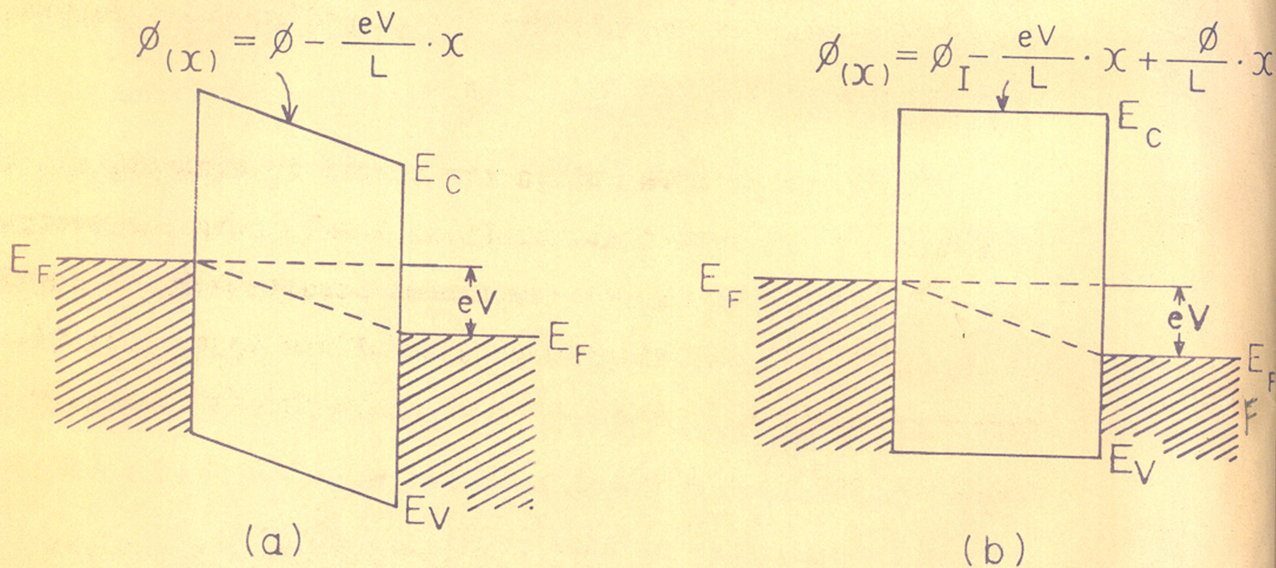


Fig.3. SCHEMATIC ENERGY BAND DIAGRAM FOR METAL-INSULATOR-METAL DIODE WITH APPLIED VOLTAGE 'V'

a) METALS OF SAME WORK FUNCTION

b) METALS OF DIFFERENT WORK FUNCTIONS

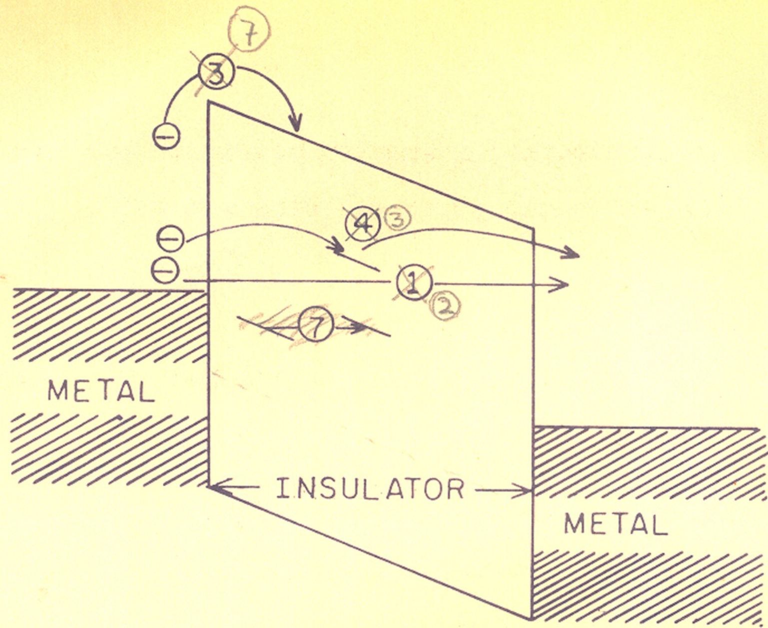
known as the work function of the metal and represents the minimum energy required to remove the electron from the metal into vacuum at $0^{o}K$.

In the case of insulators [Fig.1 (b)] we have a valence band which is fully occupied by electrons at $0^{o}K$ and a conduction band lying above, which is completely empty. The Fermi level lies in the gap separating the valence and the conduction band. The probability that a given state 'E' is occupied at a temperature T, is given by the above distribution law (equation 1). The depth of the bottom of the conduction band of the insulator from the vacuum level of the electron is called as the electron affinity and is denoted by χ_{ins}.

When two or more solids are placed in contact, electron flow takes place such that the Fermi levels equalise everywhere. Thus if we place two metal electrodes separated by an insulator, the potential energy diagram will be of two types (Fig.2), depending on whether the two metals have the (a) same, or (b) different work functions.

It can be seen that a potential barrier of height $\phi = \phi_{met} - \chi_{ins}$ is created at the metal-insulator junction.

When a voltage 'V' is applied to a metal-insulator-metal sandwich (Fig.3) the Fermi energy level in the negatively biased metal will move up by 'eV' with respect to that in the other metal. It can be seen that if two metals have the same work



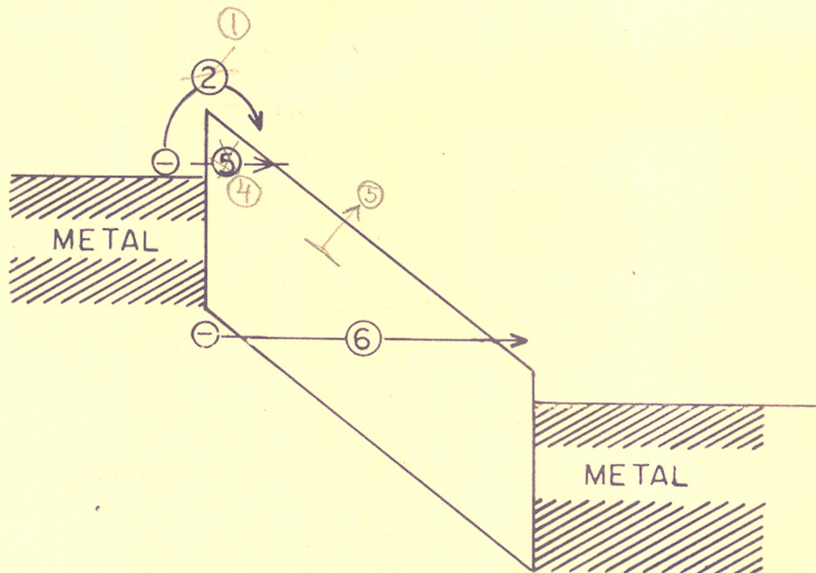


Fig. 6 SCHEMATIC REPRESENTATION OF DIFFERENT CONDUCTION MECHANISMS IN METAL-INSULATOR-METAL DIODES

function then the barrier height in the insulator will be a linear function of the distance 'x' i.e.

$$\phi_{(x)} = \phi_{met} - \frac{eV}{L} . x \qquad ...(2)$$

For metals having different work functions the contact potential $\triangle\phi = \phi_{met\ II} - \phi_{met\ I}$, will be added to the applied electrical potential 'eV' and the barrier height will change accordingly i.e.

$$\phi_{(x)} = \phi_{I} - \frac{eV}{L} . x + \frac{\triangle\phi}{L} .x \qquad ...(3)$$

We now give a brief account of the following mechanisms suggested for high current densities observed in metal-insulator-metal structures

(1) Metal to metal electron tunneling.

(2) Injection currents.

(3) Schottky field emission.

(4) Tunneling through traps.

(5) Space-charge-limited tunnel emission.

(6) Electrical breakdown.

(7) Impurity to impurity tunneling.

(8) Field ionization of traps.

Figure 4 shows each of these processes represented by an arrow bearing the corresponding index.

(1) Metal to metal electron tunneling

We have seen that the presence of an insulator between two metals gives rise to an energy barrier and according to the classical theory, it is not possible for an electron, having an energy less than this barrier, to cross from one metal to the other. The observed high current density at moderate voltages, can however be successfully explained by the quantum theory of electron tunneling. The electron wave function $\psi(x)$ decays rapidly through the insulator but if the barrier thickness is very small ($< 50 Å$) then the value of $\psi(x)$ at the other insulator-metal interface will be finite though small. Thus there is a non-zero probability of finding the electron in the other metal. This means that the electron having energy less than the barrier will penetrate through. This process of transfer of electrons from one metal to the other through the barrier is called as quantum mechanical tunneling. If no field is applied between the metals, no current will flow as the same number of electrons will flow in forward as well as backward directions. However, if we make one metal more negative than the other, then there will be a net current flow.

Tunneling has been first proposed by Frenkel[2] in 1930 and since then extensive theoretical calculations have been reported by Sommerfield and Bethe[3](1933), Holm and Kirishtein[4] (1935) and Holm[5](1954). Mead[6](1960), Fisher and Giaever[7](1961)

have reported the tunneling through $Al-Al_2O_3-Al$ diodes. The results show that the current increases exponentially with voltage and it is nearly independent of temperature as predicted by the theory. A more recent account of this effect is given by Stratton[8] (1962) and Simmons[9,10] (1963).

(2) Injection currents

The application of band theory to insulators suggests that if free carriers can be injected into either the conduction band or the valence band, then these carriers can move freely. The magnitude of the current that can be passed through a perfect insulator is limited only by the space charge of the carriers themselves, just as the space-charge limited currents in vacuum diodes. Mott and Gurney[11] (1940) have derived the relation

$$I = 10^{-13} \frac{\mu \epsilon V^2}{L^3} \qquad \ldots(4)$$

for the space-charge-limited current 'I' through the insulator.

Suitable Ohmic contacts can be made which favour electron injection into the conduction band of the insulator at the cathode and hole injection into the valence band at the anode. The one carrier injection current for holes in the valence band exhibits the same range of behaviour as the corresponding one carrier SCL currents for injected electrons. In one carrier flow, major limitations come due to traps and in the double injection case, they come from the recombination of the injected holes and electrons. The change in the life time with

the injection level also affects the current flow. Table No.1 and No.2 give the summary of the behaviour of some special cases (Lampert[12],1962).

Table No.1

One carrier SCL currents

Case No.	Description	J-V relation
i	Trap free insulator at 0^oK	$J \propto V^2/L^3$
ii	Trap free insulator with free carriers present in thermal equilibrium [12].	
	Low voltage $n \ll n_o$	$J \propto V/L$ (Ohm's law)
	High voltage $n \gg n_o$	$J \propto V^2/L^3$ (SCLC law)
	Transition voltage (Ohm's to SCLC law)	$V_{tra} = \frac{e n_o L^2}{\epsilon}$
iii	Insulator with traps[12].	
	(a) Deep (completely filled) traps[14]. No effect on current flow.	$J \propto V^2/L^3$
	(b) Shallow traps[14]. Due to trapping only a fraction of the injected carriers ($\theta < 1$) will be available.	$J \propto \frac{\theta V^2}{L^3}$
	(c) Intermediate traps[12,14]	
	Low voltage - traps are shallow	$J \propto \frac{\theta V^2}{L^3}$
	High voltage - traps become filled and act as deep traps.	$J \propto V^2/L^3$
	Trap filled limit voltage	$V_{TFL} = \frac{e N_t L^2}{\epsilon}$
	(d) Uniformly distributed traps - Filling up of traps raises the Fermi level and increases the free carrier density available for conduction. Equal increments in voltage will produce equal changes in E_F. This will give an exponential rise in the number of free carriers.	$J \propto e^{\alpha V}$

One carrier SCL currents have been reported in single crystals[15] and evaporated layers[16,17] of CdS,, single crystals of ZnS[18,19], high resistivity GaAs[20] and amorphous Se[21].

Table No.2

Double injection

Case No.	Description	J-V relation
i	Where space charge and recombination limits the double injection:	
	a) $\bar{\tau}$ independent of injection level[12,22] n_o and p_o are small, $n \simeq p$ and $\gg N_{def}$.	$J \propto \frac{V^3}{L^5}$
	b) $\bar{\tau} \left(= \frac{1}{\alpha(\bar{n})}\right)$ varies with carrier density[24] n_o and p_o are small, $n \simeq p$ and $\gg N_{def}$.	$J \propto \frac{V^2}{L^3}$
ii	Where recombination limits the double injection and space charge is relaxed through n_o and p_o.	
	a) Low voltage[12] n and p $\ll$ n_o and p_o respectively	$J \propto V$ (Ohm's range)
	b) Medium voltage[12,23] n and p are comparable to n_o and p_o	$J \propto \frac{V^2}{L^3}$ (semi-conductor range)
	c) High voltage[12,23] n and p $\gg$ n_o and p_o	$J \propto \frac{V^3}{L^5}$ (insulator range.
iii	Where life time (of hole) changes with injection level[12,24]. The insulator is thought of as having a class of recombination centres filled with electrons. The charge neutrality is maintained due to shallow donors.	
	a) Low voltage - Holes are trapped at recombination centres leading to one carrier flow.	$J \propto \frac{V^2}{L^3}$
	At the voltage threshold (V_{th}), enough trapping takes place so that the life time for holes starts increasing. As the injection level increases, more and more traps get filled and it becomes difficult to trap the holes. The hole life time thus increases considerably and the resistance falls giving rise to a current controlled negative resistance.	$V_{th} = \frac{2 \tau_{p\,low} L^2}{\mu_p}$

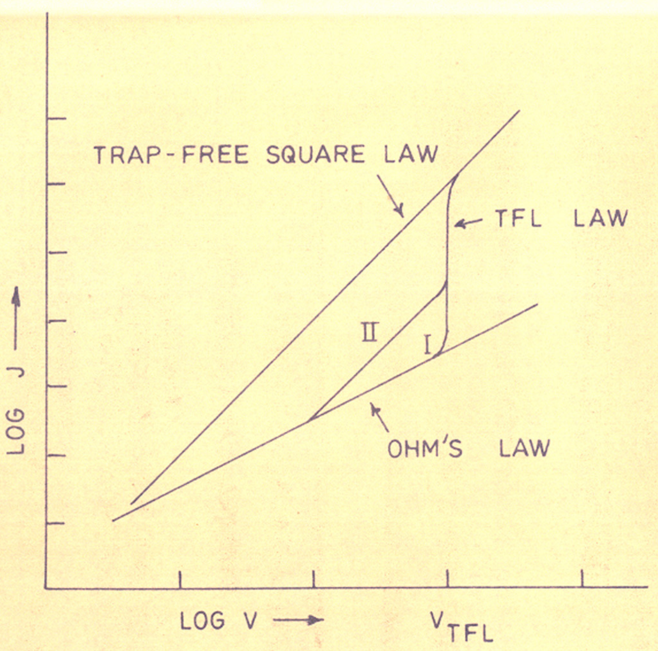


FIG. 5. LOG J - LOG V CHARACTERISTIC FOR ONE-CARRIER SCL CURRENT

I - Et - F < kT
II - Et - F >> kT

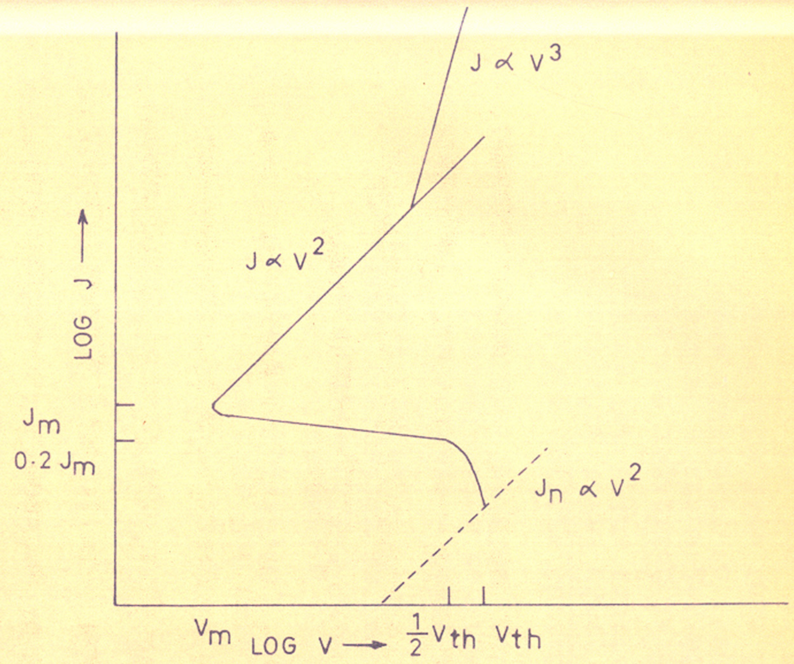


FIG. 6. LOG J - LOG V CHARACTERISTIC FOR DOUBLE INJECTION WITH UNEQUAL LIFE TIME (HOLES)

Table No. 2 .. cont.

Case No:	Description	J-V relation
b)	High voltage (i.e. after negative resistance) Double injection with n p (due to initial trapping of holes described above).	J $\frac{V^2}{L^3}$
c)	Very high voltage n and p are very large	J $\frac{V^3}{L^5}$

The results for one carrier space-charge-limited currents are summarised in Fig.5 and for double injection with unequal life time in Fig.6.

(3) <u>Schottky field emission</u>

Emtage and Tantraporn[25] (1962) have reported another mechanism of electron transport in thin insulating films namely Schottky Field Emission. According to them an electron in the metal with a forward energy greater than the potential maxima can enter the conduction band of the insulator and hence give rise to a current. The Schottky type emission is also proposed by Advani <u>et.al.</u>[26] (1960) and ~~and~~ Standy and Maissel[27] (1962).

Emtage <u>et.al.</u>[25] have observed that the films less than 100Å thick favour tunneling but thicker films show Schottky emission. Pollack[28] (1962) has reported the studies on the conduction through films ($\simeq$ 300Å thick) which show both temperature and

voltage dependence which can be explained on the basis of Schottky emission. Furthermore, he has observed that below $235^{o}K$ tunneling is more predominant than Schottky emission but above this, Schottky emission predominates. This type of conduction is also reported in mica films by Malcolm, Mccoll and Mead[29] (1965). The properties of one carrier SCL currents, tunnel and Schottky field emission can be summarized[25] as follows:

Table No.3

Mechanism	I-V dependence	I-T dependence
SCL	$I \propto V^2$	$I \propto \mu$ (mobility)
Tunneling	$I \propto V$ for $V < \phi_{met}$ $I \propto V^2 e^{-const/V}, V > \phi_{met}$	none
Schottky emission	$I = \alpha \exp(\beta V^{1/2})$	$J \propto T^2 e^{-const/T}$

where: $\beta = (e^3/kL)^{1/2}/kT$, $\alpha = AT^2 e^{-\phi/kT}$

(4) Tunneling in presence of traps

Theoretical calculations regarding the effect of impurity sites, in the forbidden gap of the insulating film, on the tunneling current have been reported by Penley[30] (1962). He has calculated tunneling currents through barriers containing one dimensional potential wells, with small effective cross-sectional areas using WKB approximation. It is assumed that the life time

of the electrons in the potential well, limits the rate at which the electrons may tunnel through the barrier. He has proposed to apply this to metal-insulator-metal diodes in which the insulator has some trapping defect states. It is shown that if the quasi-stable levels of the potential well lie near the Fermi level of the metal the current may be greatly increased by the presence of these potential wells and most of the current will flow at energies near the quasi level. Sample calculations are presented to demonstrate these features for a square well in a rectangular barrier.

(5) Space-charge-limited tunnel emission

It has been found that at high voltages, the tunnel current is much less than that predicted theoretically. Geppert[31] (1962) has explained this on the basis of space charge limitations. At very high voltages the tunneling occurs from one metal into the conduction band of the insulator. These injected carriers will in effect produce some space charge which will limit the flow of current. This is because the injected electrons will have some limiting drift velocity and we cannot increase the drift velocity i.e. the current by increasing the voltage. Thus this space charge reduces the effective applied bias.

If the traps are such that the free to trapped carriers ratio is small, this space charge effect will be pronounced. The current density also depends upon temperature as the ratio of free to trapped carriers will depend on temperature.

(6) Electrical breakdown

In insulating crystals there will be only a few electrons in the conduction band owing to the thermal excitation from impurities etc. They are too small in number to give any appreciable current at ordinary fields. At higher fields a sudden increase in current is observed. This can be attributed to an increase in the number of the electrons in the conduction band due to (a) avalanche breakdown or (b) Zener breakdown.

Avalanche breakdown

Hippel[32,33] (1931, 1932) has suggested that under the action of high field, the electrons in the lower state of the conduction band are accelerated which then transfer energy to electrons in the valence band by impact collision, raising the latter to the conduction band. The process is repeated increasing the number of conduction electrons exponentially with time as long as the field is maintained.

Hippel[34] (1938) has attributed the current increase in p-n junctions to this avalanche process. Several authors have observed such type of breakdowns in Ge and Si (McKay and McAfee[35], 1963).

Other effects of avalanche multiplication e.g. development of a stable space-charge region, the current controlled negative resistance, etc. will be discussed afterwards.

Zener breakdown

At very high fields the electron energy diagram becomes very much tilted and the electrons in the valence band have the same energy as the empty levels in conduction band elsewhere in the crystal (Fig.4) and there is a finite probability of transition from valence band to conduction band. This band to band transition is called as Zener Breakdown (Zener[36], 1934). The rate of transition was calculated using Bloch model and is given by,

$$\gamma = \frac{eFa}{h} \exp - \left[\frac{\pi^2}{h^2} \frac{maE^2}{|eF|} \right] \qquad \ldots(6)$$

where : a = lattice constant.

(7) Impurity to impurity tunneling

In the same manner as described in 6, an electron can jump from one impurity level to the other[37,38]. If, however, the energy gap between these two levels is low, it can be possible that the thermal energy will be able to transfer the electron from one to the higher level.

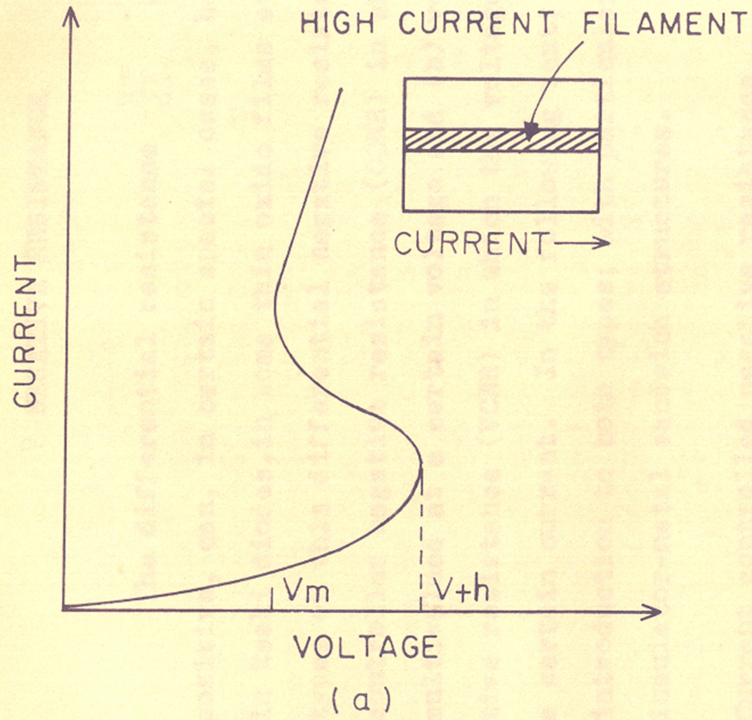
(8) Field ionization of traps

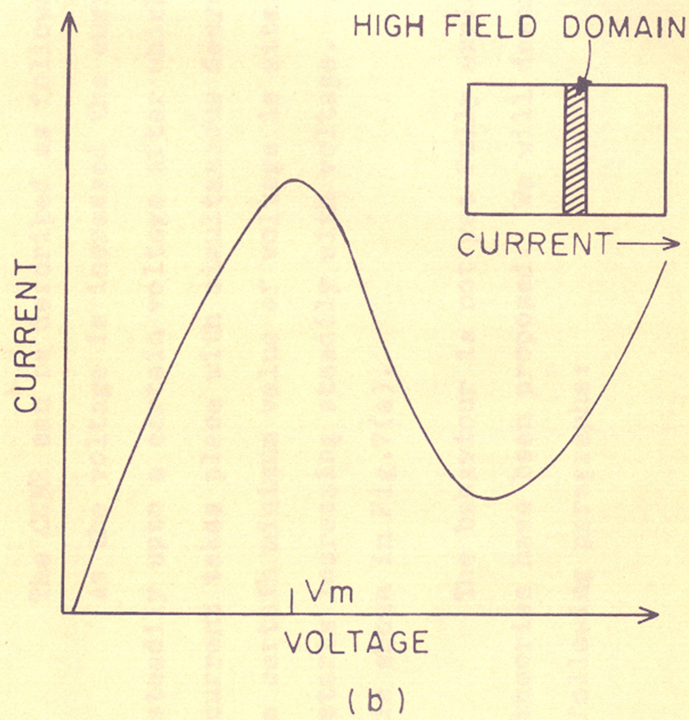
Due to high field, the shallow traps i.e. the traps near the conduction band will be ionized giving conduction electrons.

Franz[39] (1952) has shown that this is anologous to an emission from cold cathode, but without image force which gives a transition probability 'f' as

$$f = \exp\left[\frac{-4}{3} \frac{2m^*}{\hbar e} \frac{\epsilon^{3/2}}{E} \right] \qquad \ldots(7)$$

As is well-known, the carrier flow in the conduction band will depend on the scattering process but relatively its effect can be expected to be small because of very small distances involved.





(a) CURRENT CONTROLLED
(b) VOLTAGE CONTROLLED

Fig. 7. DIFFERNTIAL NEGATIVE RESISTANCE.

B NEGATIVE RESISTANCE

The differential resistance $\frac{dv}{dI}$ which is normally positive, can, in certain special cases, become negative e.g. in Esaki diodes, in some thin oxide films etc. There are two types of this differential negative resistances (Fig.7), (a) current controlled negative resistance (CCNR) in which the current is multivalued at a certain voltage and (b) voltage controlled negative resistance (VCNR) in which the voltage is multi-valued at a certain current. In the following text, we are giving a brief introduction to both types; with particular reference to metal-insulator-metal sandwich structures.

(I) Current controlled negative resistance

The CCNR can be described as follows:

As the voltage is increased the current first increases steadily upto a certain voltage after which a sudden increase in current takes place with simultaneous decrease in voltage. After a certain minimum value of voltage is attained the current again starts increasing steadily with voltage. A general I-V curve is shown in Fig.7(a).

The behaviour is not yet fully explained and a number of theories have been proposed. We will describe them in the following paragraphs:

Avalanche injection

Gunn[40] (1956) has introduced the idea of avalanche breakdown to explain the CCNR. At the voltage V_{th} where the sudden increase of current starts, the avalanche ionization[41] [Arthur et.al. (1956)] begins and additional carriers so produced slow down the increase in voltage but their space charge leads to a field distortion, the field near the anode being considerably larger than the mean field. After increasing the current to higher state the field is confined to a very thin region near the anode and the field in the entire region is reduced to nearly zero. This avalanche region is now a prolific source of holes and we can draw more current at a low field which is confined to this region.

Chopra[42] (1963) has observed a similar CCNR in niobium oxide films. In general, he has observed a rise in current which is first linear and then exponential. At higher voltages there is a rapid rise in current giving an intrinsic breakdown. A stable CCNR is observed at low temperatures. Furthermore, he has observed that the breakdown voltage increases while the current density reduces on decreasing the temperature. The symmetrical behaviour rules out any injection phenomenon. Some observations such as multiple negative resistances and hysteresis have been explained on the basis of traps. At 78°K the current

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in pre-negative resistance region obeys V^2 dependence and in the post-negative resistance region the current obeys the law $I = I_o e^{\alpha\sqrt{V}}$ which is similar to Townsend discharge equation. In general, he has concluded that the phenomenon is a bulk property and the relation $I \propto e^{\alpha\sqrt{V}}$ indicates some multiplication mechanism.

He[43] has reported a similar negative resistance (CCNR) in thin CdS films sandwiched between gold electrodes. First, there is a non-symmetrical CCNR on the rectifying side which later transforms into a symmetrical characteristic at higher current density. The impact ionisation of the impurities or traps is supposed to start the avalanche which is responsible for carrier multiplication. This is supported by the relation $I \propto e^{\alpha\sqrt{V}}$.

The mechanism of avalanche breakdown has also been used by him[44] (1965) to explain the CCNR in thin oxide films. He has studied the oxides of Ta, Nb and Ti of thickness from 50-500Å, with second electrodes as Al, Ag, Au, etc. He has proposed that the space charge set up by the slow moving holes redistributes itself in such a way that it occurs across a thin critical region capable of maintaining the avalanche. This explains the negative resistance in the "reverse" direction of the rectifying structure. It has been further concluded that the breakdown voltage is inversely proportional to the dielectric constant. The study of the capacitance as a function of voltage suggests the existence of a critical thickness.

Double injection with change in hole life time

Lampert[24] (1962) has suggested a mechanism for CCNR on the basis of double injection. He has assumed that the insulator contains acceptor like levels which lie below the Fermi level and for which $\sigma_p \gg \sigma_n$ (σ = capture cross section). It is shown that at a critical voltage V_{th}, the hole life time increases considerably and double injection current starts. Then the current increases and the voltage drops down to

$$V_m = (\sigma_n n / \sigma_p p) \; V_{th}$$

giving the CCNR. The presence of traps gives rise to sensitivity to light and hysteresis in the I-V curve.

Geppert[45] (1963) has observed a symmetrical CCNR and spontaneous oscillations in Nb-Nb_2O_5-Me structures, which he has attributed to the double injection with unequal life time.

According to Lampert[24] the oscillations are due to dominance to the negative resistance over the circuit resistance and if the oscillations are not permitted then the CCNR would be observed.

Avalanche breakdown double injection

Steel et.al.[46] (1962) have studied the I-V characteristics of a forward biased p-n junction. He has concluded that the existence of minority carriers in the body of the diode is essential. According to him the negative resistance is due to the two carrier current that follows the onset of avalanche

breakdown at the point contact. The role of avalanche breakdown is to furnish a copious supply of minority carriers for injection at the point contact. The reduction of voltage i.e. the negative resistance is a consequence of the fact that the current in the bulk following the breakdown at the point is a two carrier current which is carried at lower voltage than if it were a pure majority carrier current.

Injection mechanism

Beam and Armstrong[47] (1964) have proposed a mechanism where an impact ionization of the metal ions is supposed to be caused by the carriers injected into the oxide by Schottky field emission or tunneling. This explanation has been questioned by Chopra[44] on the basis of his experimental results.

Ridley[48] (1963) has discussed the inherent instability associated with a specific differential negative resistance. In the case of current controlled negative resistance high current filaments are formed and in the case of voltage controlled negative resistance high field domains are formed. These domains are generally mobile. The sizes of these filaments and domains are governed by the size of the specimen and the least entropy production principle. The effect of an external circuit is to inhibit stable filament formation in the case of current controlled negative resistance and to impose conditions under which VCNR will be observed due to stable domain formation.

(a) Voltage controlled negative resistance

The VCNR can be described as follows:

The current first increases steadily with voltage upto a critical point beyond which an increase in voltage reduces the current. After a certain minimum value, the current again starts increasing steadily with voltage (Fig.7 b). Sometimes a saturation is also observed before the current drops down.

Kromer[49](1958) has used the fact that the high kinetic energy electrons and holes in semiconductor have negative masses. The contribution due to these carriers will show a negative effect. If the concentration of such carriers is increased i.e. at high fields, the negative resistance in the I-V characteristic will be observed. He has suggested that this region of the I-V curve could be used for oscillators and amplifiers.

Ridley and Watkins[50](1961) have suggested that the carriers, at high electrical fields, can be transferred into sub-bands higher in the conduction band. Due to large mass in this sub-band, the mobility will in effect decrease and this will give rise to voltage controlled negative resistance under some special conditions. Si and some III-V semiconductors have been predicted to show these effects. Certain "electrical domain" formation has also been proposed.

They[51](1961) have pointed out that at high fields the capture rates for electrons and holes with the repulsive charged centres increase. This alters the steady state density of

carriers which gives a situation in which the free electron carrier density decreases giving rise to voltage controlled negative resistance. The effect is expected to show in n-Ge doped with Cu, Ni and Au.

Hilsum[52] (1962) has further discussed the possibility of achieving negative resistance by transferring electrons into a higher sub-band in a system in which there are two minima separated by a small energy. The lower minimum is associated with low mass than the upper one. The mobility decreases at high fields at which the transfer takes place from one to the other sub-band showing the negative resistance. Calculations are presented for GaSb & GaAs.

Ridley and Pratt[53] (1963) have observed a bulk differential negative resistance due to electron tunneling through an impurity potential barrier in gold doped germanium. The electric field causes the electrons to tunnel to the repulsive trap centres whose capture cross section increases with field. This in effect is supposed to give the bulk differential negative resistance. The speciman splits into high field and low field domains.

Barraud[54] (1963) has studied the behaviour of gallium arsenide at high electric field. The I-V characteristic shows ohmic region upto 800 v/cm. then the current decreases and oscillations are observed at 3000 v/cm. Further increase in voltage gives a rapid increase in current after 3000 v/cm. A mechanism involving the trapping centres has been given to explain the negative resistance and the oscillatory behaviour.

The theory of Gunn effect[55] (1963) and its relation to the voltage controlled negative resistance have been discussed by Krömer[56] (1964) on the basis of the Ridley-Watkin's and Hilsum's models.

Hickmott[57] (1961) has studied aluminium oxide films of 150-1000Å thick, grown by anodic oxidation method. He has observed that as the voltage is increased there is a small increase in current at 4.1 volts and then on lowering the voltage a pronounced VCNR region is observed. He has explained the increase in the current at 4.1 volts due to a positive dipole formation caused by the field ionization of metal donors. The decrease in current after current maximum is suggested to be due to increased barrier for ionization (ϕ minimum). The trapping of the carriers at voltage sensitive traps and the decrease in their life time have been suggested to be responsible for decrease of the current.

Pollack *et.al.*[58] (1963) have studied the conduction through vacuum deposited aluminium oxide thin films sandwiched between metal electrodes. A forming process as reported earlier by him[28] has been used to increase the electronic transfer from metal to insulator. He has explained the I-V behaviour on the basis of an ionic space-charge layer similar to that suggested by Geller[59] (1956). After this forming process is complete, a negative resistance in the I-V characteristic is observed only when the applied voltage is decreased from higher than $\simeq$ 3 volts.

The current peak occurs at 3 volts irrespective of the temperature but the magnitude of the peak current decreases on decreasing the temperature. The phenomenon is slightly different from that observed by Hickmott[52] earlier.

Hickmott[60] (1963) has discussed the mechanism for the electron emission in Al-Al_2O_3-Au diodes. Thermoionic emission and emission of electrons having some extra energy of about 2 volts in oxide conduction band have been suggested.

A very typical behaviour similar to that observed by Pollack[28] has been reported by Mukherjee and Allan[61] (1964) in Al-Al_2O_3-Se-Au sandwich cells. When the gold electrode is positive and the voltage is increased, the sample shows a VCNR in absence of light. However, when the voltage is decreased no VCNR is observed, nor is it observed when the gold electrode is made negative.

Hickmott[62] (1964) has studied the impurity conduction and negative resistance in thin anodic oxide films. The study of thickness effect has shown that the negative resistance is nearly independent of the oxide film thickness. The effect of electrode material and temperature on the development of conductivity and on the VCNR has been studied. The observations have suggested that the impurities in the film play an important role. Furthermore, if the voltage is kept below V_M the temperature effect is not so pronounced which shows that the conduction at low voltages is not governed by thermally activated processes. The idea of the formation of an impurity band close to Fermi level has been invoked to explain the results.

With a view to study the mechanism of the VCNR Hickmott[63] (1964) has prepared diode structures with SiO films of thickness between 150-1500Å and has measured the potential distribution across the film. The study has shown that after the development of VCNR, a high field region of 120Å thick develops near the negative electrode. When a reverse voltage is applied, the VCNR is observed but the potential distribution is slightly altered. A phenomenological model involving the formation of an impurity band has been proposed. The ionization from the impurity band gives electrons into conduction band giving rise to increased conductivity as the voltage is increased. In addition, another competitive process is visualised to exist, in which the tunneling into this impurity band from valence band or some impurity level neutralizes these ionised sites. The rate of the second process rises exponentially with respect to the applied voltage, hence at high voltage it dominates over the first and a combined effect is to give the VCNR.

Smith[64] (1962) has reported a saturation in dark currents of semiconducting CdS and GaAs at 1600 v/cm. field strength, which gives the drift velocity of 300 cm/volt sec., which is equal to the sound velocity in crystal. The saturation has been explained to be due to the transfer of energy of the electrons to the accoustic waves or phonons. The

observed current oscillations have been explained as follows: When the drift velocity of electrons exceeds the sound velocity the accoustic waves in the crystal gain energy from this and a growing hypersonic wave is generated giving oscillations. Hutson[65] (1962) has used the same principle to explain non-ohmic behaviour in piezoelectric semiconductors and bismuth.

Three types of current instabilities have been observed by Ismau Kuru[66] (1965) in n-GaAs. One which occurs at highest voltage is the Gunn effect. The other two are related to each other. The I-V curve shows VCNR between 65°K and 85°K. At temperatures higher than 85°K current saturation has been observed and incoherent microwave emission has been reported. The cause for the low field instabilities has been proposed to be due to accoustic phonon excitation by the electron drifting through the crystal with a velocity as small as 7 x 10^{5} cm/sec. or less.

Current oscillations after a saturation in current in n-GaAs at low temperatures have been reported by Yamashita and Rivo[67] (1966). In addition a hysteresis in the I-V curve near the saturation region is also observed. The above observations together with the potential distribution study have been explained on the basis of trapping of high field domains in the conductivity minimum region of the sample.

VCNR in semiconductors due to accousto-electric instability has been proposed by E'pshtein[68] (1966), Ioffee[69] (1966), Pemidenkov et.al.[70] (1966), while high field domain formation has been given by Bonch[71] (1966), Ihanova et.al.[72] (1966) and Boer[73] (1965) to explain it.

A VCNR, only with one polarity has been reported by Mead and Spitzer[74,75] (1963, 1964) and explained on the basis of the Fermi level position at the metal-semiconductor interface.

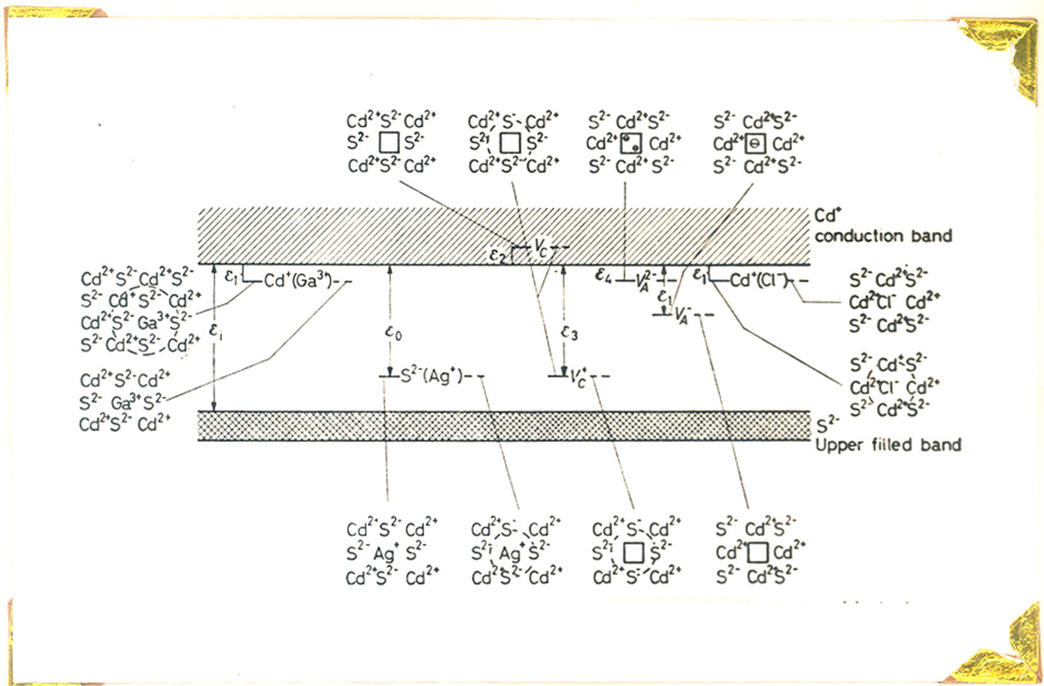


Fig : 8 : Schematic energy band diagram of CdS with defects states and impurity levels. The full lines represent the occupied and the dotted lines represent the unoccupied levels.

GENERAL PROPERTIES OF CADMIUM SULPHIDE

Cadmium sulphide is a semiconductor with a band gap of 2.45 e.v. The crystal structure is hexagonal.[76] The unit cell dimensions are $a = 4.131 \mathring{A}$, $c = 6.691 \mathring{A}$, $c/a = 1.62$, $Z = 2$. Cd ions occupy the $000;\ \frac{1}{3}\frac{2}{3}\frac{1}{2}$ sites and S ions $00\frac{3}{8};\ \frac{1}{3}\frac{2}{3}\frac{7}{8}$. Each Cd^{++} atom is surrounded tetrahedrally by S^{--} and vice versa. Kröger et.al.[77] (1954) have studied the electronic properties of cadmium sulphide single crystals and have proposed an energy band diagram in which the corresponding energy levels due to some foreign atoms (Cl, Ga) and due to the possible non-stoichiometry in the composition is presented (Fig.8).

The vacuum deposited films are usually polycrystalline with only one degree orientation making all basal planes(001) parallel to the substrate. The resistivity and the colour of the film changes according to the stoichiometry of the film. The films are generally n-type and this is suggested to be due to excess cadmium which can be controlled by the deposition conditions.

Dresner and Shallcross[78] (1963) have studied the crystallanity and electronic properties of evaporated CdS films on glass substrates kept at 170°C (degassed at 400°C prior to deposition) at 10^{-5} torr. Polycrystalline (hexagonal) n-type CdS films are obtained.

Zuleeg and Senkovits[79] (1963) have developed a vapour deposition method for CdS films and studied the properties of such films. Zuleeg and Muller[16] (1964) have reported that the deposited films have α-CdS phase and consist of crystallites oriented with their 'c' axis normal to the substrate. Furthermore, n-type character and conductivity ranging from 1-100 Ω cm. have been reported. Mobilities of the order of 10-50 cm^2/V sec. are observed. An impurity level at .12 e.v. from the conduction band has been proposed which is due to sulphur vacancies as slight dissociation during evaporation is expected to take place.

Foster[80] (1963) has discussed the vacuum deposition methods. The n-type behaviour has been explained. The vapour pressure of sulphur is 10^{-5} torr at room temperature and above and that of cadmium approaches this value only at $150^{\circ}C$. So depositions at vacuum above 10^{-5} torr with substrate at room temperature give excess cadmium. Furthermore, he has suggested some post-deposition heat treatments to remove this excess cadmium e.g. (1) heating in inert atmosphere or in vacuum, (2) reacting with H_2S and (3) compensating with impurities like Ag and Cu.

A cubic phase has been reported[81] in CdS films deposited on freshly cleaved muscovite mica ($250^{\circ}C$) from a Knudsen-cell-vapour source ($870^{\circ}C$).

In general the vacuum deposited CdS films are polycrystalline and n-type.

We have seen that there is a barrier at the metal-semiconductor contact. If the height of this barrier is very small, free carriers can be injected into the respective bands of the semiconductors. This type of contact is called Ohmic contact. If this barrier is high then the metal gives a blocking contact to the semiconductor.

Learn[82] et.al.(1966) have studied the potential barrier heights for various vacuum deposited metal-CdS film contacts. The CdS films are deposited at 10^{-6} torr on substrates at 175°C and are n-type. In, Al and Cr are observed to give Ohmic contacts while Pt, Au, Pd, Ni etc. give blocking contacts. Table No.4 gives the barrier heights for different metal-CdS contacts. A comparison is made with the respective values for single crystals

Table No.4

Contact potential for metal-CdS injection

Metal	Barrier heights in ev.			
	Single crystal		Polycrystalline film[82]	
			Initial	Post-heated
Pt	0.85[83]	1.2[84]	0.61	0.88
Au	0.77	0.68	0.60	0.77
Pd	-	0.60	0.50	0.67
Ni	0.45	-	0.30	0.50
Cu	0.30	0.45	0.40	0.75
Ag	-	0.37	-	-
Al	Ohmic	0.26	Ohmic	Ohmic
In	"	Ohmic	"	do
Ga	"	"	"	do

Several authors have studied the conduction through films of n-CdS. The electron injection from Ohmic contact gives SCL currents, while that from blocking contact gives the Schottky emission. An extensive study has been done by Zuleeg and Muller[16] (1964) on Au-CdS-In diodes. It has been shown from the I-V & I-L dependence that the injection from the In contact gives SCL behaviour while the capacity-voltage and current-voltage relations show that the injection from gold is Schottky emission type. SCL currents have been observed earlier by Dresner and Shallcross[17] (1961) in vacuum deposited films.

Extensive studies have been made on the negative resistance in single crystals of CdS. A voltage controlled negative resistance in the current-voltage characteristic has been observed and explained on the basis of high field domain formation, tunneling through impurity barrier and accuosto-electric instability[54,68-73,86,87] at critical fields. A typical CCNR has been observed by Chopra[43] (1963) and explained on the basis of avalanche injection mechanism. A detailed account of these studies is given earlier. A meta-stable conduction band lying in the energy gap in evaporated films of CdS has been reported by Brodle and Eastman[85] (1965).

Microwave emission from n-CdS illuminated by a mercury lamp or a He-Ne laser in strong electric field has been reported by Masao Miya and Masatoshi Teri[86] (1966). This has been thought

to be due to the piezoelectric coupling between conduction electrons and accoustic phonons in the crystal. Similar oscillations have been observed with a non-uniform illumination. In the I-V plot, a voltage region (before the oscillations start) is observed in which the I-V variation is neither Ohmic nor saturating.

A VCNR in I-V curve of CdS has been reported by Yamamato and Kenji[87] (1966). The I-V curve departs from Ohmic property beyond a critical voltage (Ea) and shows a peak value (Eb). These voltages become larger for high conductivity. The VCNR is observed only below $-50^{o}C$. The monochromatic light affects the current peaks by shifting to high fields. A mechanism of piezoelectric field caused by building up of accoustic waves is thought to be responsible for the behaviour.

CHAPTER - II

E X P E R I M E N T A L

CHAPTER - II

EXPERIMENTAL

A. PREPARATION OF BASIC MATERIALS

CADMIUM SULPHIDE

(i) Preparation by precipitation

Pure cadmium sulphide powder was prepared by the following method. Pure sulphuric acid (5N) was added drop-wise to cadmium carbonate (CP) solid till all the solid dissolved completely. The solution was then diluted with distilled water and filtered. The filtrate was boiled with bromine water for about 20 minutes. Liquor ammonia was then added drop-wise till the precipitate which formed first, got dissolved again. A gelatinous precipitate of iron and some other impurity hydroxides, however, did not dissolve and was removed by filtration. Hydrogen sulphide gas was prepared in a Kipp's apparatus and was purified by passing successively through (i) dilute hydrochloric acid solution to dissolve any iron impurities, (ii) distilled water, (iii) several stages of saturated barium hydroxide solution and finally again through distilled water. The purified H_2S was passed through the filtrate, obtained above, for about 2-3 minutes, at a rate of 1 bubble a second. After this partial precipitation, the solution was filtered. H_2S was then bubbled through the filtrate for a

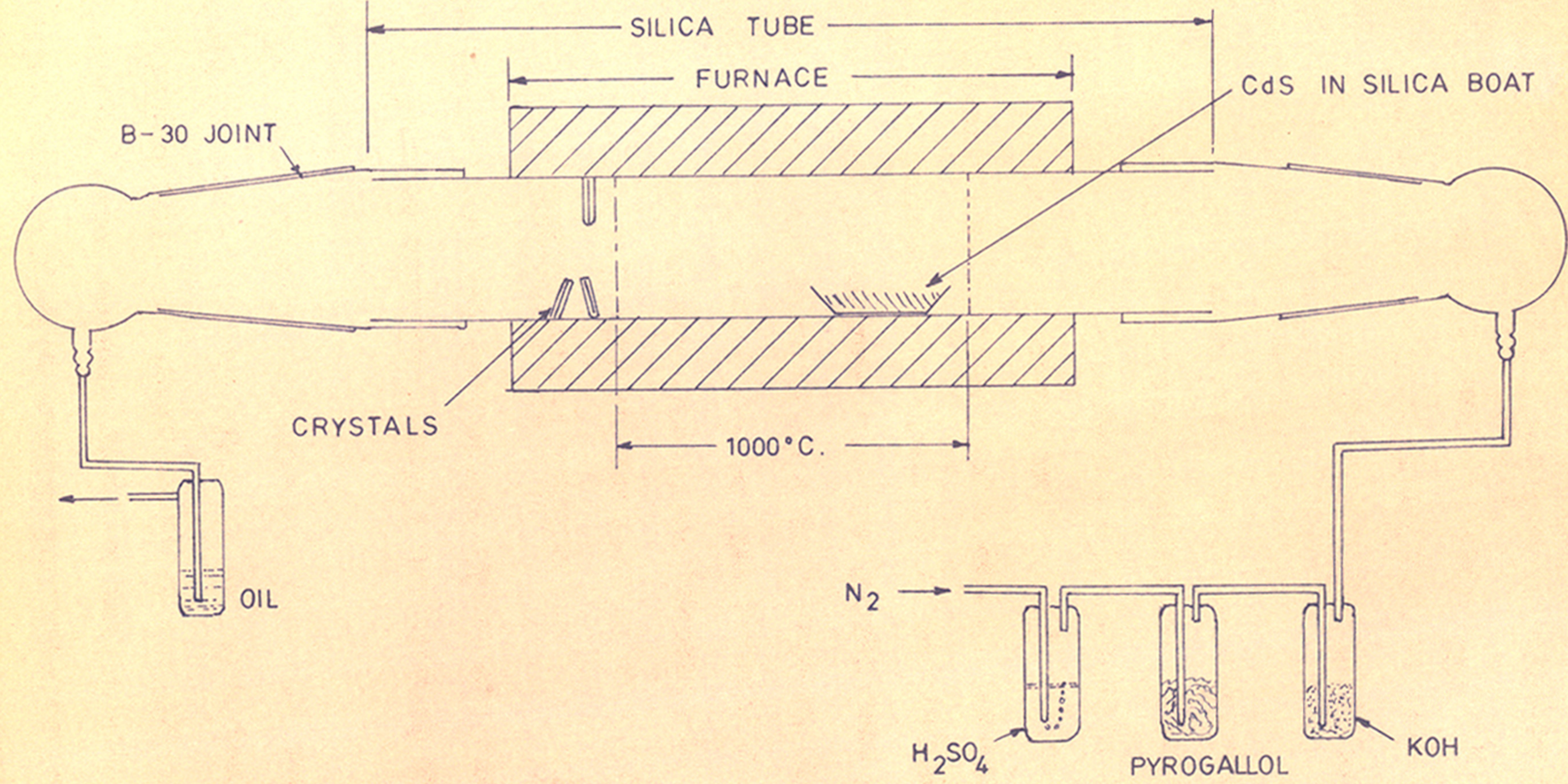


FIG. 9. FURNACE FOR CADMIUM SULPHIDE SINGLE CRYSTALS GROWTH

long time till the precipitation was complete. The orange-yellow precipitate of cadmium sulphide was washed with hot distilled water several times to remove any soluble impurities. Sufficient care was taken to avoid any contamination during the whole process. The precipitate was then removed and dried at 80°C. This cadmium sulphide was powdered and used for further experiments.

Cadmium sulphide samples supplied by M/s. Riedel(orange CP) and by L. Light and Co.(99.99% pure) were also used.

(ii) Preparation of pellets

Cadmium sulphide in the form of small pellets was found useful for the vacuum deposition process and was therefore prepared by the following method. The powder, after grinding in an agate mortar was pressed in a die, made of die steel. All the parts coming in contact with the powder were highly polished to avoid any impurity contamination in successive pressing operation. The pressing was performed on a Carver Laboratory Press fitted with a calibrated pressure gauge. A pressure of 6000 p.s.i. was applied. The pellets prepared were normally of 1 cm. diameter and 2 mm. thick. These pellets were cut to proper sizes (about 1 x 0.2 x 0.2 cm.) so that they could be introduced easily into the tungsten spiral used for the deposition.

(iii) preparation of cadmium sulphide single crystals

Single crystals from these powders were prepared by a method similar to that used by Stanley[88] (1956). A silica tube furnace as shown in Fig.9 was used. Cadmium sulphide powder was kept in a silica boat. Initially the furnace was flushed with nitrogen gas purified by passing through an alkaline

pyrogallol solution and finally dried over potassium hydroxide pellets. After flushing out, the rate of nitrogen was kept approximately 50 cc./min. The furnace was then heated slowly to 1000°C. The temperature of the furnace was measured with the help of a calibrated chromel-alumel thermocouple, the top of which was located very close to the boat. The entire heating operation took about 10 hours. The furnace was kept at 1000°C for 20 hours and the rate of nitrogen flow was kept constant throughout the process. After about 20 hours, the temperature was decreased very slowly to 400°C and then the rate of cooling was increased. It took about 10 hours to cool from the highest temperature down to the room temperature. Crystals, mostly of needle shape, grew on the sides of the furnace tube. The crystals were removed carefully and were used as the source for the deposition of CdS.

(iv) Preparation of doped cadmium sulphide

Cadmium sulphide doped with In_2S_3 or Ag_2S in different proportions was prepared by the following procedure:

(a) Preparation of In_2S_3

About 2 grams of indium metal (99.99% pure) was dissolved in ~~the~~ AR nitric acid. The solution was evaporated to dryness on a sand bath. The indium nitrate crystals were dissolved in distilled water and the solution was filtered. Purified hydrogen sulphide was bubbled through this solution with constant stirring. The yellow precipitate of In_2S_3 was washed with distilled water and dried at 80°C.

(b) Preparation of Ag_2S

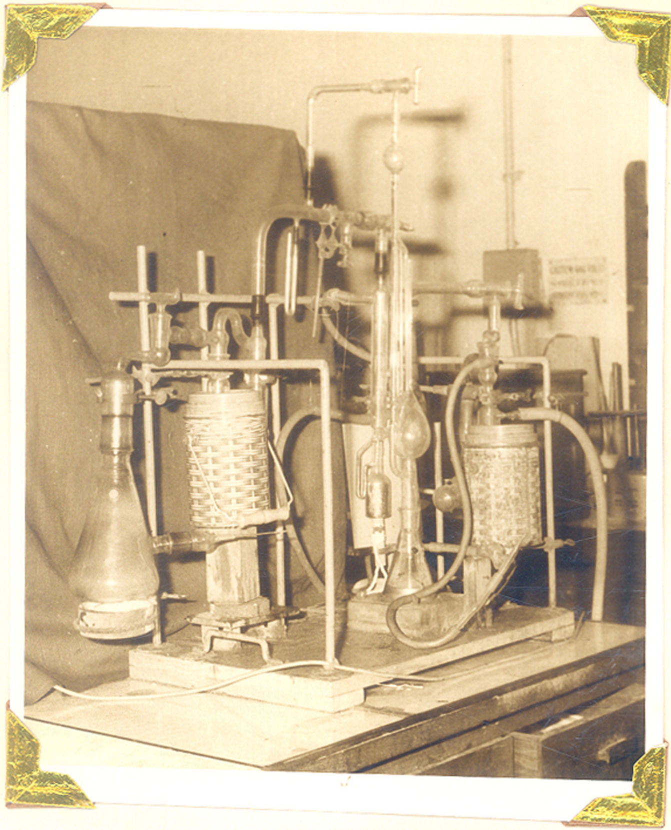
About 5 gms. of $AgNO_3$(AR) was dissolved in distilled water and then purified hydrogen sulphide was bubbled through this solution. The black precipitate was removed, washed with distilled water and finally dried at $80^{o}C$.

(c) Preparation of mixtures

Weighed quantities of cadmium sulphide (dry powder) and corresponding quantity of Ag_2S or In_2S_3 were mixed in an agate mortar with distilled absolute alcohol. The pellets from the dried mixture were prepared as described earlier. These pellets were then reacted in a silica tube furnace at $700^{o}C$. An atmosphere of dry purified hydrogen sulphide gas was maintained during the reaction. Finally the pellets were cooled in H_2S atmosphere and were then used as source material for cadmium sulphide depositions. The following table gives the different mixtures used:

Table No.5

Mixture No.	Mixture Type	Cadmium sulphide taken gms.	In_2S_3 added gms.	Ag_2S added gms.
1	N1	5.0128	0.1035	-
2	N_2	5.0122	0.2545	-
3	N_3	5.0172	0.5196	-
4	N_4	5.0205	0.9984	-
5	P_1	5.0260	-	0.0962
6	P_2	5.0060	-	0.2524
7	P_3	5.0025	-	0.5074
8	P_4	5.0000	-	0.9998



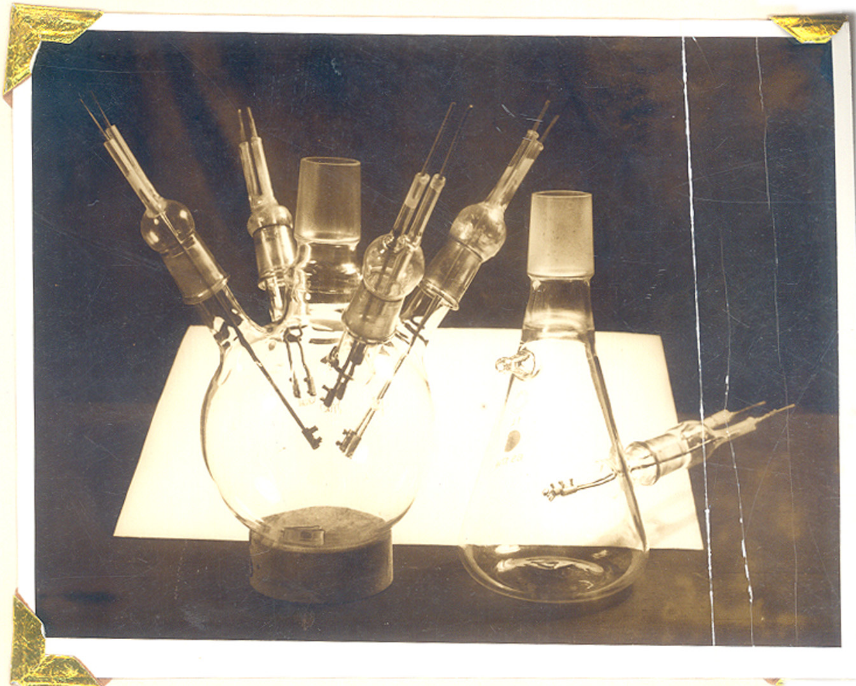
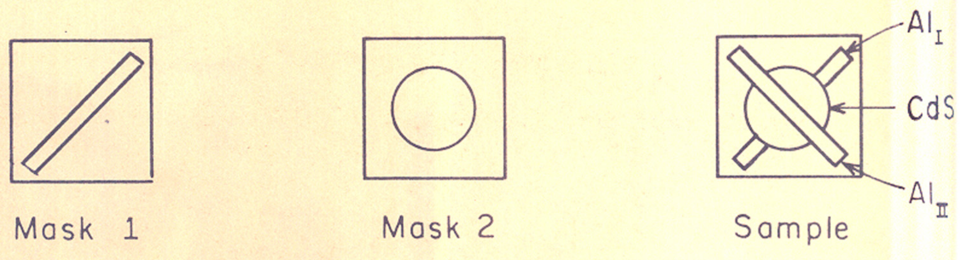
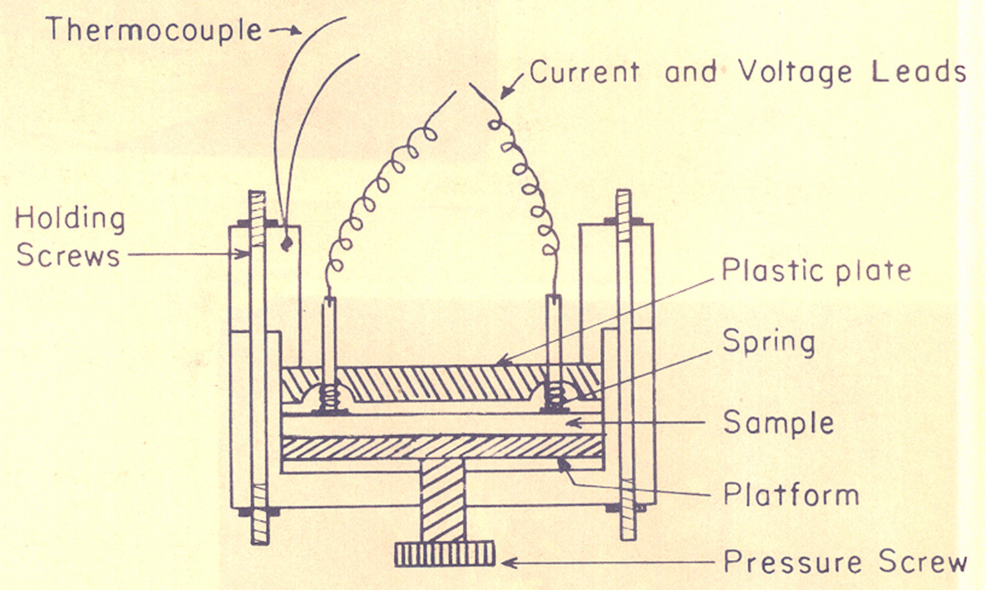


Fig : 10 : Vacuum unit and deposition glass chambers.



MASKS AND SAMPLE



SAMPLE HOLDER

Fig. 11. MASKS, SAMPLE AND SAMPLE HOLDER

METALS

Aluminium (specpure), indium (99.99%), gold (99.9%) and copper (99.9%), were used for preparing the metal electrodes.

B: PREPARATION OF SAMPLES

1. Vacuum deposition unit

An all-glass vacuum unit (Fig.10) was built in the laboratory (capable of giving a vacuum of the order of 10^{-6} torr). An oil-rotary pump capable of giving a vacuum of 10^{-3} torr to 10^{-4} torr was used as a backing pump. This was connected to a drying tube (containing P_2O_5 in a glass boat), through a cold trap containing ice and salt freezing mixture. This was followed by the mercury diffusion pump. Pressure measurements were done with the help of a previously calibrated McLeod gauge. This vacuum pump assembly was connected to the deposition chamber through a liquid air cold trap. A stopcock was provided to release the vacuum between the diffusion pump and the McLeod gauge.

2. Preparation of the metal-CdS-metal sandwich samples

The metal-cadmium sulphide-metal sandwich structures were prepared by depositing metal, cadmium sulphide and metal sequentially on a thoroughly cleaned microscope glass slide. Proper masks were used to give a crossed structure as shown in Fig.11. Two types of masks were used: Mask No.1 was pre-

prepared by making a diagonal slit of 2.5 x 0.25 cm. size in a metal piece of 2.5 x 2.5 cm. size. Mask No.2 had a circular hole of 1.5 cm. diameter at the centre of a similar metal piece.

(a) Preparation of substrate

Microscope slide made of glass of size 2.5 x 2.5 cms. was used as the substrate. The slide was cleaned thoroughly with chromic acid and was then washed with distilled water. Further cleaning was achieved by dipping the slide in a detergent solution for about half an hour after which it was removed and rinsed with distilled water several times and dried carefully.

(b) Deposition of metal electrodes

For metal deposition, the glass slide cleaned as above, was covered with mask No.1. This was then placed at the bottom of a conical flask having a B-45 male joint fixed to its mouth. A tungsten filament was connected to two copper metal electrodes, passing through a B-29 female joint fitting on a B-29 male joint, provided on the side of the conical flask. These copper electrodes were sealed to the joint with araldite. The tungsten filament was clamped firmly to the ends of the copper electrodes (Fig.10). The distance between the filament and the substrate was kept at about 5-6 cms. The metal to be deposited was kept in the tungsten filament in the form of a wire or a thin metal strip. The deposition chamber was then connected to the vacuum unit. The backing pump was started and evacuation was continued for about 10-15 minutes. When a vacuum of 10^{-3} - 10^{-4} torr was obtained, the mercury diffusion pump was started and was continued for 1-2 hours when a vacuum of the order of 10^{-6} torr was

obtained. The tungsten filament was then heated electrically. The current through the filament was controlled with the help of a variac and measured by an ammeter connected in series. The temperature of the filament was previously calibrated with respect to the input current by measuring the temperatures with the help of an optical pyrometer (Cambridge Instrument Co. Ltd.) at various current values through the tungsten filament. The current was increased slowly till the metal in the filament melted and then increased further till the metal started evaporating. The following table summarises the conditions used for the deposition of various metals.

Table No.6

Condition for metal deposition

No.	Metal	Description of filament	Evacuation time at 10^{-6} torr	Temp. of deposition °C
1	Al	Two tungsten wires(30 swg) were twisted together and a spiral was made	2 hours	1150
2	In	Single wire of tungsten (30 swg) was used to make a spiral	2 hours	995
3	Au	-do-	1-1/2 hrs.	1465
4	Cu	-do-	1-1/2 hrs.	1270

3. Deposition of cadmium sulphide

(a) Deposition under normal conditions

After the metal deposition was over the deposition assembly was dismantled. The slide was removed from the chamber. Mask No. 1 was replaced by Mask No.2. A deposition assembly similar to the one described above was used for deposition of cadmium sulphide films. The masked slide was introduced in the chamber with a separate filament assembly as described above. The cadmium sulphide pellets (for pure and doped samples) or crystals (for pure samples only) were kept in the tungsten filament and the deposition unit was assembled. This was connected to the vacuum unit through the B-45 joint. The system then was evacuated for 10-15 minutes by the backing pump only, after which the diffusion pump was started. When a vacuum of the order of 10^{-6} torr was reached, further evacuation was continued for half an hour. During the evacuation the cadmium sulphide source was baked at about 200°C, by heating the filament. This was necessary to remove any of the trapped gases which gave difficulty in deposition due to spurting. After this baking process was over, the diffusion pump was stopped. After half an hour the vacuum dropped to 10^{-3} - 10^{-4} torr. The filament temperature was then increased upto 900°C. The temperature was controlled by monitering the current through the filament as described earlier. The evaporation was started and continued till the cadmium sulphide was evaporated completely. The thickness of the cadmium sulphide film was about 0.1 μ- 2.0 μ.

(b) Deposition at various filament temperatures

Depositions were carried out at various filament temperatures by following the above procedure except that the filament temperature during the different experiments was varied between 750-950°C. This was achieved by passing a fixed current which could be measured by an ammeter in series. The deposition was continued till all the material was evaporated.

(c) Deposition under different vacuum conditions

The deposition was carried out under three different vacuum conditions.

(i) At a vacuum of the order of 10^{-3} - 10^{-4} torr, following the procedure described above (a).

(ii) At a vacuum of the order of 10^{-6} torr. Here the same procedure was followed as described above upto the baking stage. After the baking was over the diffusion pump was not stopped, so that the vacuum was of the order of 10^{-6} torr. The deposition was carried out ~~at this order of vacuum~~ as described earlier.

(iii) In an atmosphere of sulphur vapour of the pressure of the order of 10^{-6} torr. For this purpose solid sulphur was filled in a tube, plugged with a piece of cotton wool and introduced in the deposition chamber, adjacent to the sample. Apart from this, the procedure was the same as described in (ii) above.

During all the above described processes the substrate was not heated; a slight heating due to the radiations from the filament ~~source~~ could not however be avoided.

(d) Deposition on hot substrate

For this purpose, a different deposition chamber (spherical) was used (Fig.10). There were four symmetrical electrode assemblies similar to that described earlier. A B-45 male joint was fused at the top. First of these four electrode assemblies was used for connecting the leads for the heating filament. The second was used for the tungsten filament for cadmium sulphide deposition. The third one was used so as to connect the previously calibrated chromel-alumel thermocouple. Fourth one was kept as a spare.

A heating element for the substrate heating was prepared as follows. A nichrome resistance tape was wound around a thick mica piece of size slightly greater than that of the sample. The two ends of this nichrome tape were clamped with clips. The wound element was sandwiched between two mica sheets to provide the electrical insulation. The two leads were connected to the electrodes inside the deposition chamber.

The deposition of CdS was done as follows. First, the heating element was connected to the fitted electrode assembly No.1. Then the thermocouple leads were connected to the electrode assembly No.3. The glass slide, over which the first metal electrode was deposited, was mounted on the heating filament, the deposited side was facing upwards. Mask No.2 was then placed over this in the appropriate position. The

thermocouple was then placed in close contact with the mask. The whole substrate assembly was then inserted in the chamber. After adjusting the position of the substrate at the bottom of the chamber, the electrode assembly No.2, with cadmium sulphide in the filament, was put in position and the chamber was then connected to the vacuum unit. The pumps were started in the right sequence and when a vacuum of the order of 10^{-6} torr was attained the substrate heating was started and was continued for one hour. During the last half an hour, the baking of cadmium sulphide was also started. The current through the substrate heating element was controlled so as to give substrate temperature of 50°C, 100°C, 150°C and 200°C. When the respective temperatures were reached, further heating was continued for 20 minutes for the stabilization of temperature. After this, the cadmium sulphide was deposited in a vacuum of the order of 10^{-6} torr as described on page 41. After the complete deposition, the substrate was allowed to cool slowly to room temperature. The vacuum was then released and sample was removed.

(e) Second metal deposition

After cadmium sulphide was deposited by one of the above described procedures the second metal was deposited by using the same procedure as described for the first metal. The conical deposition chamber was used. A crossed structure (Fig.11) was obtained by using mask 1 in proper orientation.

(f) Deposition without intermediate exposure to air

During the procedures for fabrication of metal-cadmium sulphide-metal sandwich structures, air had to be let in into the chamber to make proper arrangements such as change of masks and filaments etc. This exposure to air might form a very thin layer of oxide or leave some adsorbed gases in between the two deposited layers. So a second set of samples was prepared by the following technique which avoided this type of exposure at least at one of the two semiconductor-metal interfaces.

The deposition was carried out in the chamber having four electrode assemblies. To one electrode assembly, a tungsten filament containing aluminium was fixed. The second electrode assembly, diametrically opposite of this was fitted with another tungsten filament containing cadmium sulphide. The other two electrode assemblies were fitted with small mica sheets to mask the filament containing aluminium and that containing cadmium sulphide.

The cleaned glass slide was placed at the bottom of the chamber with mask No.1 fitted on it. First, aluminium was evaporated to give the bottom electrode. The whole assembly was then allowed to cool down in vacuum. The baking of cadmium sulphide was started (10^{-6} torr) and continued for half an hour. The deposition of CdS was then done at 10^{-3} - 10^{-4} torr as described earlier. After complete evaporation the air was let in. The assembly was dismantled

and the glass slide was removed. The same mask was readjusted so as to give a crossed structure. The second metal electrode (aluminium) was then deposited in the conical deposition chamber. Thus the interface between the first metal and the sulphide was not exposed to air while that between the cadmium sulphide and second electrode was exposed.

To protect the second CdS-metal junction from exposing to air the same arrangement as described above was used. First, aluminium (bottom electrode) was deposited on a cleaned glass slide by using mask No.1 in the conical deposition chamber. Air was let in, the assembly was dismantled and the glass slide was removed. The mask was then adjusted to give cross-structure. The next two depositions namely that of the cadmium sulphide and of the top aluminium were done in the spherical chamber. The slide was introduced and adjusted. The chamber with the four electrode assemblies was connected to the vacuum unit as described above. However, in this case the cadmium sulphide deposition was carried out first and then the top aluminium electrode was deposited. Here the interface between cadmium sulphide and top aluminium electrode was not exposed to air but that between the first metal and cadmium sulphide was exposed.

(g) <u>Preparation of oxide layer on aluminium</u>

A thin film of aluminium oxide was grown on the bottom aluminium by its oxidation. The deposited aluminium glass-slide was kept in a glass tube shown in Fig.12. A current of dry oxygen was passed over the film. The tube was kept in a round

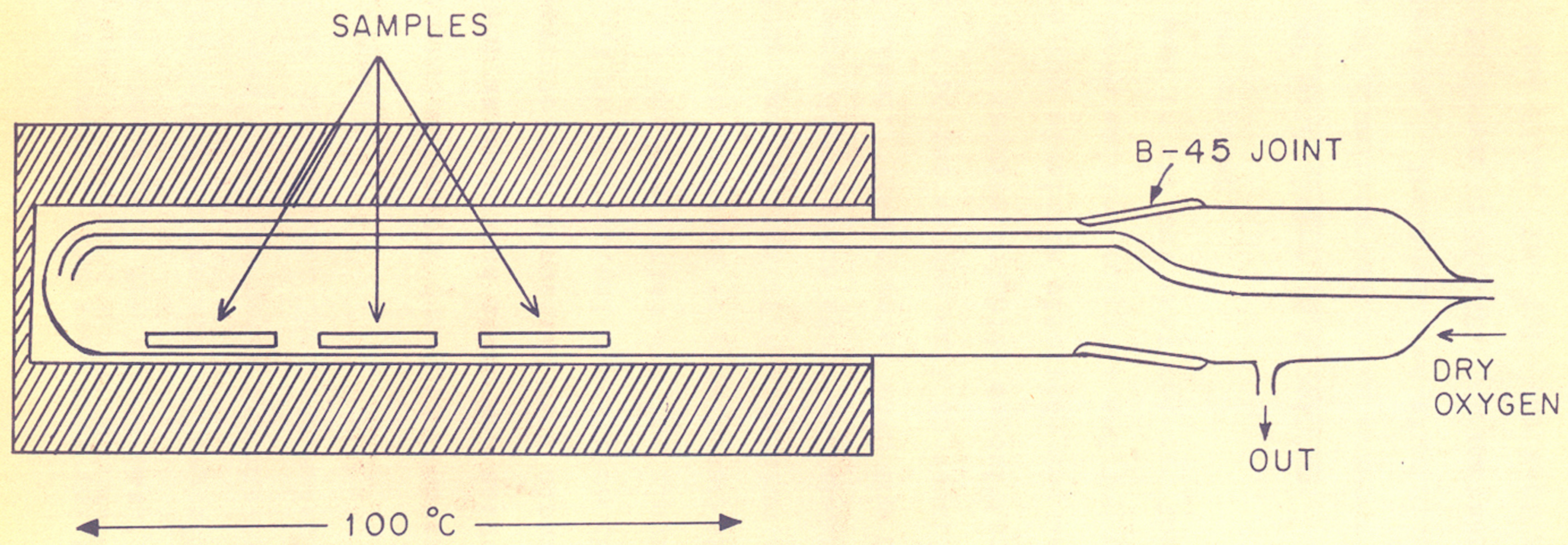


Fig. 12. FURNACE FOR OXIDATION AND HEAT TREATMENTS

furnace and the temperature near the slide was maintained at 100°C. The oxidation was continued for 6 hours. During this time aluminium oxide thin film was grown and the approximate thickness is expected to be 20-30Å.

(h) Post-deposition treatments on cadmium sulphide films

After the cadmium sulphide film had been deposited on the first metal electrode at pressures of 10^{-3} - 10^{-4} torr and on cold substrate, it was heated at 300°C for four hours in

(i) sulphur

(ii) vacuum (10^{-3} torr)

to see the effect of these treatments on the I-V characteristics of the final Al-CdS-Al structures. In all the cases the tubular furnace described above (Fig.12) was used. Sulphur atmosphere was obtained by keeping some solid sulphur in the cooler parts of the tube ($\simeq 80$°C) and its vapour was carried over by the flowing nitrogen (or the furnace was evacuated using a water suction pump with a P_2O_5 drying trap in between). Furthermore, samples were also prepared by first heating in vacuum and then in sulphur atmosphere. The second electrode was then deposited on the top to form a crossed structure.

C : MEASUREMENTS

Thickness

The film thickness was measured by weighing the sample before and after the deposition of film. Only the average thickness could be obtained by this method.

Current voltage characteristic

(i) Contacts

For the study of the current voltage characeristic of these diodes at room temperature, press contacts were used. A thin cleaned aluminium foil was placed on the metal electrode film. A crocodile pin with a soldered flat jaw was used for pressure contact. Copper wires were soldered to these crocodile pins and used as measurement leads.

To study the current-voltage characteristic at various temperatures a brass sample holder as shown in Fig.11 was used. The sample was kept on a metal plate with the deposited side facing upwards. Contacts to the metal film were made by keeping a plastic plate having four holes, in which soldered contacts to the metal films were pressed by means of small springs. A calibrated copper-constantan thermocouple, the junction of which was located in a well, drilled in the sample holder, was used to measure the temperature. The complete sample holder assembly was then inserted in a pyrex tube. The tube was placed in a thermos flask containing liquid air. The I-V characteristic was measured when the sample attained a constant temperature. After some time the liquid air evaporated

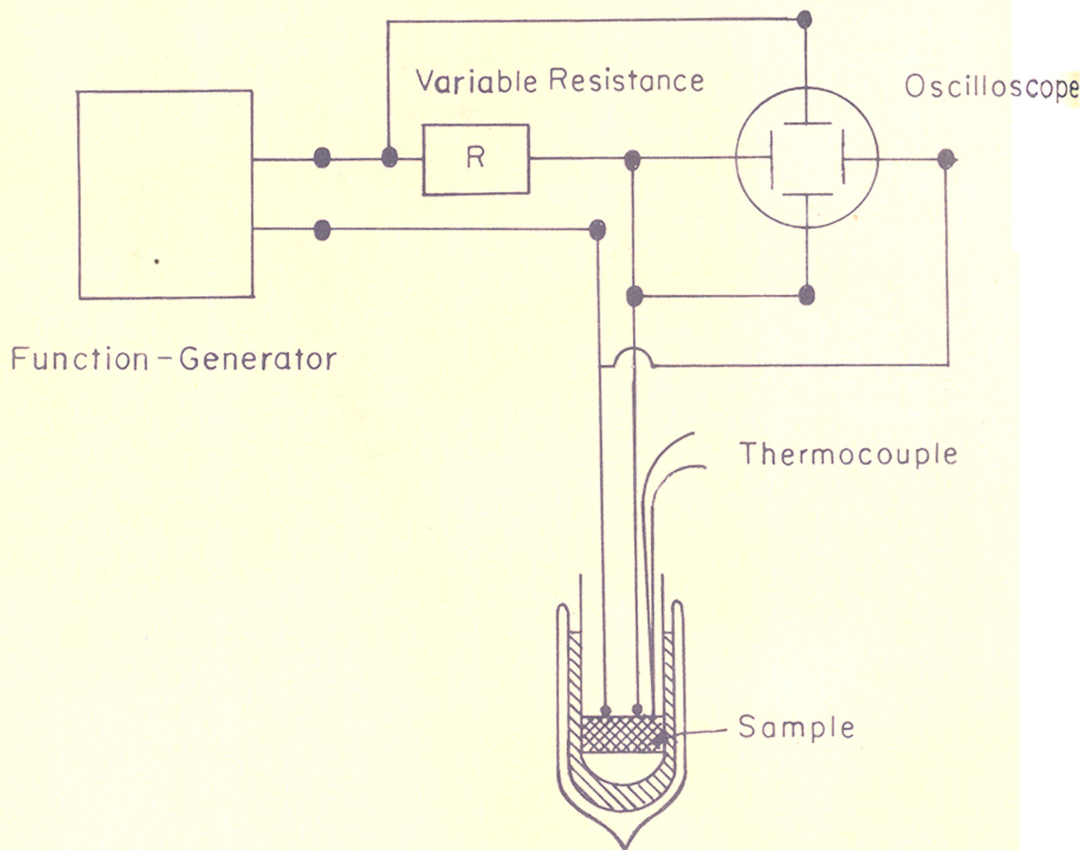


Fig. 13. MEASURING CIRCUIT

and the sample temperature started increasing slowly. The rate of rise of temperature was about $\frac{1}{2}$°C per minute, so that I-V characteristics could be measured at different intermediate temperatures with reasonable accuracy. For measurements at higher temperatures, the sample holder assembly, with the tube, was placed in hot water, maintained at different temperatures in the thermos flask.

(ii) Circuit

A simple circuit as shown in Fig.13 was used. An ARLAB low frequency function generator type OS 1 was used as a power source. The frequency variation range was 1/400 to 1/0004, c/sec. Three types of functional forms, the square, triangular and sine, could be used. A 12-volt battery with a variable potentiometer was also used when high current densities were needed. A Tektronix Type 515 oscilloscope was used as a recorder. The voltage across the sample was measured on the horizontal axis (X axis). The current through the sample was measured as follows. The voltage developed across a standard resistance, in series with the sample, was applied to Y (vertical) plates. This voltage was converted into corresponding current value 'I' by the formula:

$$V = I R$$

where 'V' is the voltage developed across the standard resistance R.

(iii) Calibration of the oscilloscope

The oscilloscope was calibrated with the help of the square wave calibrated output, supplied with the oscilloscope. The calibration was done for both X axis as well as Y axis.

Measurements

The photographs of the I-V characteristics on the oscilloscope were taken with the help of oscilloscope camera (D. Shackman & Sons, London and Chesham) fitted with the oscilloscope permanently. The photographs were taken on 35 mm. films. For low frequency measurements the exposure time was equal to the time taken to complete one cycle. For high frequency measurements the exposure time was 1/2 second. The exposed films were removed and developed by using a contrast developer and fixed in 'hypo' solution. After washing with running water they were dried and used for enlarging and printing.

CHAPTER - III

R E S U L T S

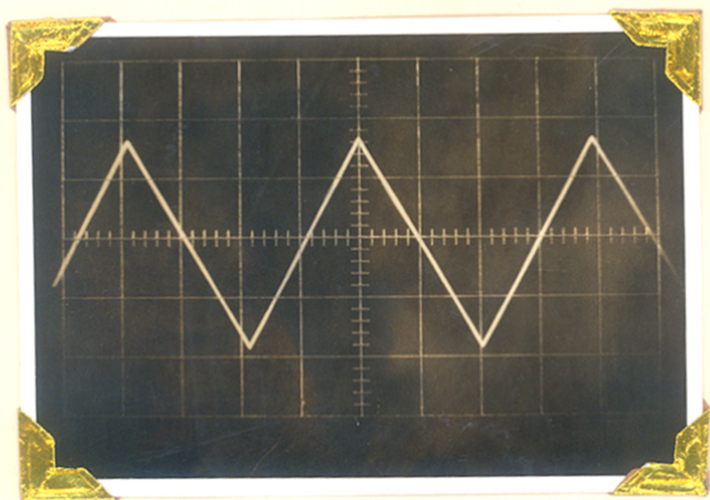


Fig : 14 : Applied pulse characteristic with repitition frequency 0.25 c/s.

X - 5 small divisions per second. Y - 4 small divisions = 1 volt.

CHAPTER - III

R E S U L T S

A : STUDY OF Al-CdS-Al STRUCTURES

Samples of aluminium-cadmium sulphide-aluminium sandwich structures have been prepared by depositing thin films in the above sequence on a clean microscope glass slide. The cadmium sulphide film ($\simeq 1.5\,\mu$ thick) is deposited on the substrate at room temperature in a vacuum of the order of 10^{-3} - 10^{-4} torr with the source at about 900°C. The current voltage characteristics of these structures at room temperature show two stages. The first is a pre-breakdown stage in which the structure shows a higher resistance and the second is the post-breakdown stage where the resistance is about 1/4 to 1/5 of that in the pre-breakdown stage. When the voltage in the first stage is increased beyond a critical value V_x, the structure transforms irreversibly into the second stage in which a dual negative resistance is observed. In both the pre-breakdown and post-breakdown stages, a non-linear dependence of current on voltage is obtained. In what follows, we describe these two stages in detail.

(1) Pre-breakdown stage

Figure 15 shows the room temperature current-voltage characteristic in the pre-breakdown stage for Al-CdS-Al sandwich structure. Triangular pulses of frequency 0.2.5 c/sec. have been used (Fig. 14). Most of the samples are found to

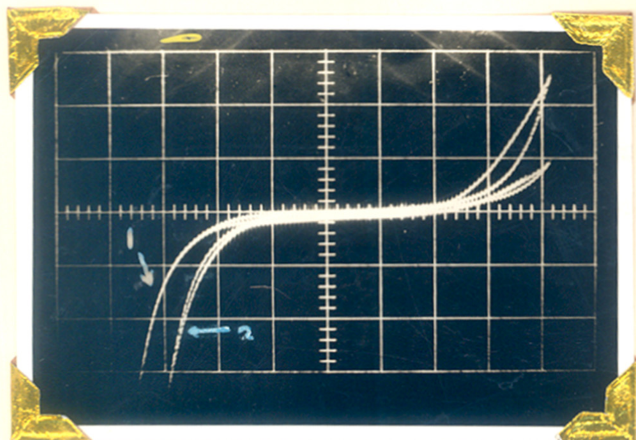


Fig:15: Aging effect on I-V characteristic of Al-CdS-Al diode in the pre-breakdown stage:

(1) Initial curve (2) Taken after 5 minutes

X - 4 small divisions = 1 volt Y - 4 small divisions = 5

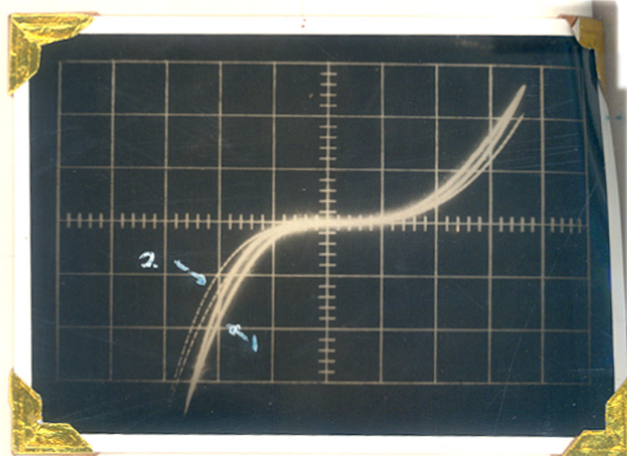


Fig.16: Effect of frequency on I-V characteristic of Al-CdS-Al diode in the pre-breakdown stage.

(1) Repetition frequency 0.025 c/s (2) Repetition frequency 0.25 c/s

X - 4 small divisions = 1 volt Y - 4 small divisions = 5 a

show higher resistance and hysteresis when the top electrode is made positive (upper right hand quadrant in Figure 15). During the other half of the cycle in which the top electrode is negative, the resistance is smaller and the hysteresis is nearly absent. From Fig. 15 we can also see that the current varies non-linearly with voltage. Figure 15 also shows some aging effect. The curve marked (2) is taken after subjecting the sample for 5 minutes to a voltage cycling between ± 2.5 volts. The curve marked (1) is the initial curve. We can clearly see that the current density decreases on repeated cycling. The original curve (1) is not restored even after keeping the field off for several hours.

Figure 16 shows the effect of frequency (0.25 and 2.5 c/sec.) of the applied voltage on the I-V characteristic. The increase in the frequency decreases the current density in both the directions. If the field is kept on at 2.5 c/sec., the current density keeps on reducing continuously to lower values. Furthermore, it takes several hours to come to its original conductivity state after the field is switched off. If the duration of the applied field is long then the original conductivity stage is not restored. In most of the samples the current on low resistance side falls more rapidly than that on the other side and after some time the rectification observed in Figure 15 vanishes completely.

The above mentioned behaviour is maintained as long as the applied voltage does not exceed a certain critical voltage V_x, the value of which depends upon the nature, thickness and

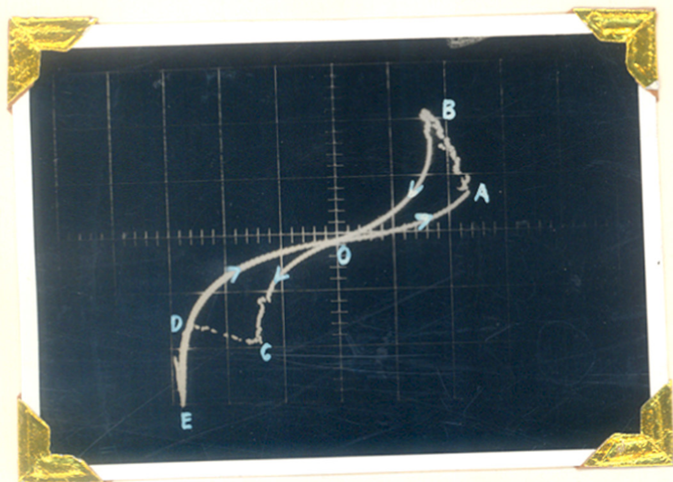


Fig: 17 : I-V characteristic of Al-CdS-Al in the post-breakdown stage.
X - 4 small divisions = 1 volt. Y - 4 small divisions = 5 ma

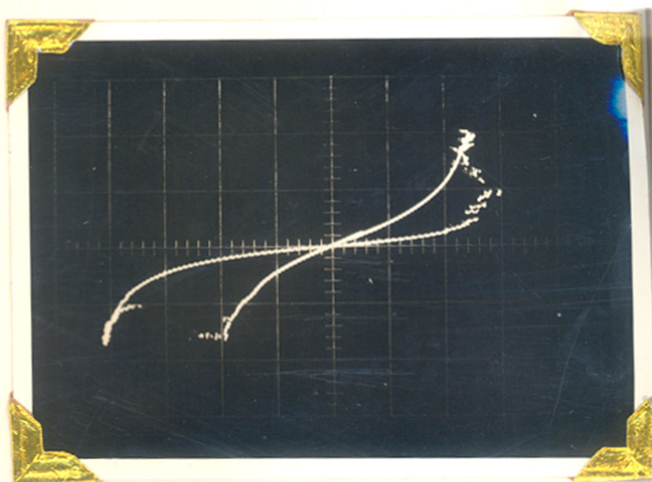


Fig: 18 : Steps and current saturation in the I-V characteristic of Al-CdS-Al diode in the post-breakdown stage.
X - 4 small divisions = 1 volt. Y - 4 small divisions = 5 ma

temperature of the cadmium sulphide film. If the applied voltage is increased beyond this point (V_x) an irreversible breakdown takes place. In most of the samples this is observed first on the high resistance side and then on the other side. After this breakdown is complete, the structure transforms into the second (or post-breakdown) stage characterised by a dual negative resistance.

(2) Post-breakdown stage

After the above mentioned irreversible transformation, the structure shows at room temperature a current-voltage characteristic as shown in Fig.17. Triangular pulses (Fig.14) of frequency 0.25 c/sec. have been applied. In this stage, when the applied voltage on the top electrode (positive) is increased from zero (point O), the curve follows the path OA. At voltage V_A (point A) the current starts increasing i.e. the sample is transformed into a high conductivity state. During this transition, the voltage across the sample drops down to a value V_B and the current increases from I_A to I_B. This transition is slow and irregular but sometimes, clear steps are observed (Fig.18). After the transformation is complete, on decreasing the applied voltage from V_B, the same conductivity state (i.e. high conductivity state) is maintained and the curve $B'BO$ (i.e. different from OAB) is traced out. If we decrease the voltage beyond zero (i.e. top electrode negative) a path symmetrical to that of BO is obtained upto the point C (voltage V_C). At C, the curve drops down to a lower value through an increase in voltage to the point D(voltage V_D). Here the transition from high conductivity state to low conductivity state takes place. This transition is smooth and more rapid

than the low to high conductivity state transition. However, sometimes discreete steps similar to those in the other transition are also observed (Fig.18). In some samples near the transition point V_C, a small current saturation is observed (Fig.18) and in this part of the curve, sometimes random oscillations are also observed. After this low conductivity transformation is complete, further increase in voltage does not change the state (curve DE in Fig.16). When the voltage is decreased from V_E, the path EOA is traced out i.e. the sample remains in the low conductivity state.

This process can be described as follows: From voltages V_O to V_A a low conductivity state is maintained, at V_A an increase in the current through a decrease in the voltage to V_B takes place and the structure goes to high conductivity state. This high conductivity state is maintained till a critical voltage V_C is reached at which the current decreases through an increase in voltage and the structure switches back to the low conductivity state. This state is maintained till we reach V_A and the whole pattern is retraced. The part OABO of the curve resembles the current controlled negative resistance region with large hysteresis effects i.e. the path $\overrightarrow{OB}$ is not same as $\overrightarrow{BO}$. The path OCDEO resembles a voltage controlled negative resistance region with high hysteresis effects i.e. the path $\overrightarrow{OC}$ is not the same as $\overrightarrow{CO}$. So in the same sample both current controlled as well as the voltage controlled negative resistance characteristics are observed and hence the name "Dual Negative Resistance".

In both the states (i.e. the low conductivity as well as the high conductivity state) the current varies non-linearly with voltage. The current controlled negative resistance is observed only when the top electrode is positive and the sample is initially in the low conductivity state and the voltage controlled negative resistance appears only when the top electrode is negative and the sample is in the high conductivity state to start with. These sides correspond to the high resistance and low resistance sides in the pre-breakdown stages. Furthermore, this switching of the conductivity states takes place at the respective critical voltages V_A and V_C only. If, on the other hand, the applied voltage is kept below these critical voltages, the switching over is not observed. For example, if we are in the low conductivity state and the positive voltage on the top electrode is increased from V_0 to (Fig.16) voltage say V_A' ($< V_A$) and we then start decreasing the voltage, the switching from low to high conductivity state does not take place even if we cross the point E in the curve i.e. the same state is maintained and a path OA'OEO is traced out without any transition or hysteresis. As we go nearer to V_A the distortion starts. Similarly, if we are initially in the high conductivity state and a voltage is applied such that we never cross V_C (say upto V_C') the path OC'O is retraced. Even if we go to the other side i.e. if we make the top electrode positive and we come to the point V_B, no transition will take place and the curve OC'OBO will be traced out backwards and forwards without hysteresis and any negative resistance characteristic.

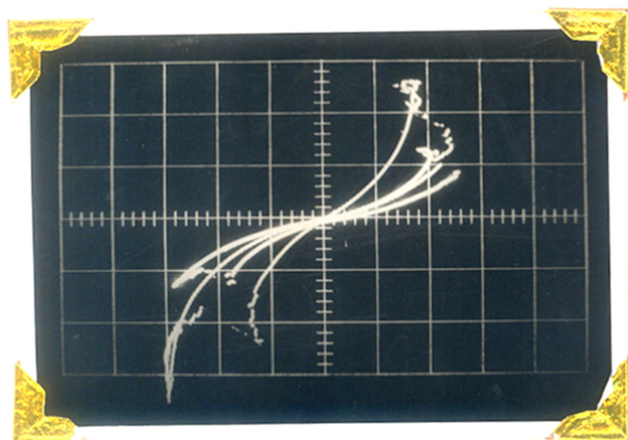


Fig: 19 : I-V characteristic of Al-CdS-Al diode with incomplete transformation.

X - 4 small divisions = 1 volt. Y - 4 small divisions = 5 ma

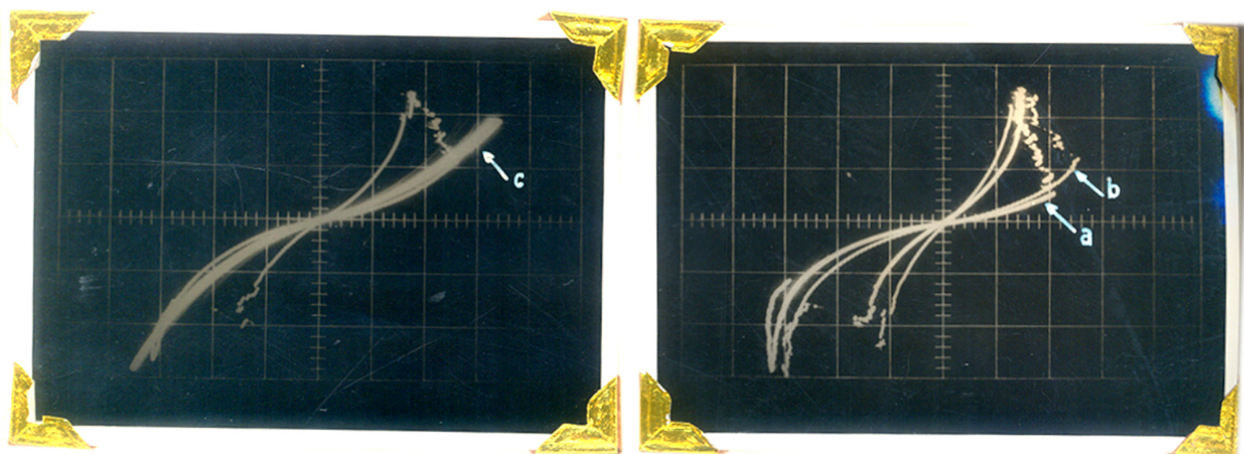


Fig: 20 : Effect of frequency on I-V characteristic of Al-CdS-Al diode in post-breakdown stage.

(a) Repetition frequency 0.0025 c/sec.
(b) Repetition frequency 25.00 c/sec.
(c) Repetition frequency 250.00 c/sec.

X - 4 small divisions = 1 volt. Y - 4 small divisions = 5 ma.

It is also observed that the transformation from low to high conductivity state is slow. Furthermore, if we control the voltage such that this transformation is not completed, i.e. the final value I_B is not reached, then the value of V_B is higher than that in the samples which are completely transformed (Fig.19). However, in all the samples $|V_B| \simeq |V_C|$ regardless of the fact that complete transformation from low to high conductivity state has occurred or not. It was not possible to interrupt the voltage during the transition from high conductivity to low conductivity state because this transition is much faster. Furthermore, $I_B \leq I_C$ in every sample.

At low frequencies (even down to 0.001 c/sec.) no appreciable change in the general behaviour is observed except that the voltage V_A is a little less and the transformation becomes more irregular [the curve (a) in Fig.20]. At higher frequencies ($\simeq$250 c/sec.) the low conductivity to high conductivity transformation is incomplete because of its slowness and the observed behaviour is as shown in Fig. 20, curve (b). The values of voltage V_A and V_D increase as the frequency is increased. Furthermore, the voltage V_B mostly remains equal to V_C for frequencies upto 25 c/sec. They differ slightly at higher frequencies. At very high frequencies of the order of 250 c/sec. the negative resistances vanishes completely and the curve is similar to the low conductivity curve at low frequencies (Fig. 20, curve C).

B : EFFECT OF ELECTRODE

With a view to find out whether this dual negative resistance phenomenon is observed when metals other than aluminium are used as electrodes, Me-CdS-Me sandwiches have been prepared with indium, gold and copper metal electrodes in place of one or both the aluminium electrodes and their I-V characteristics studied.

Aluminium and indium have been observed to give ohmic contacts to the deposited cadmium sulphide films while gold and copper are known to give blocking or rectifying contacts[82]. It is also well-established that the vacuum deposited cadmium sulphide films are always n-type and so the majority carriers are electrons[80]. Furthermore, the ohmic contacts give space charge limited currents while the blocking contacts give either the tunneling or Schottky field emission. The study of the effect of metal electrode on the current voltage characteristic is useful to establish some aspects of conduction mechanism in both the pre-breakdown and post-breakdown stages.

The following three configurations are studied:

(1) <u>Both electrodes are ohmic</u>

(a) Al-CdS-In
(b) In-CdS-Al
(c) In-CdS-In

(2) <u>One of the two electrodes is ohmic</u>

(a) Al-CdS-Au and Au-CdS-Al
(b) Al-CdS-Cu and Cu-CdS-Al

(3) Both electrodes are blocking

(a) Au-CdS-Au

(b) Cu-CdS-Cu

Both electrodes ohmic

The three sandwiches (a), (b), (c) show the same behaviour as Al-CdS-Al structure discussed earlier. The high resistance and hysteresis are observed when the top electrode [i.e. indium in (a) and (c) and aluminium in (b)] is positive. In the post-breakdown stage the dual negative resistance is observed. The voltages V_B and V_C remain nearly the same as in Al-CdS-Al structure but V_A and V_B are slightly increased. It is also observed that during the CCNR path, patches due to burning are sometimes formed on indium film and if the cycling is continued for a long time, the indium film gets destroyed. Secondly, the transition from high conductivity to low conductivity state (VCNR) is faster than that in the Al-CdS-Al structure.

In general, in all these structures the pre-breakdown stage irreversibly transforms into a second stage where the dual negative resistance is exhibited. The CCNR is observed when the sample is in the low conductivity state and the top electrode is positive irrespective of the elctrode metal Al or In.

One electrode ohmic

Under this class, we have studied the sandwiches where aluminium is used as the ohmic metal electrode because indium

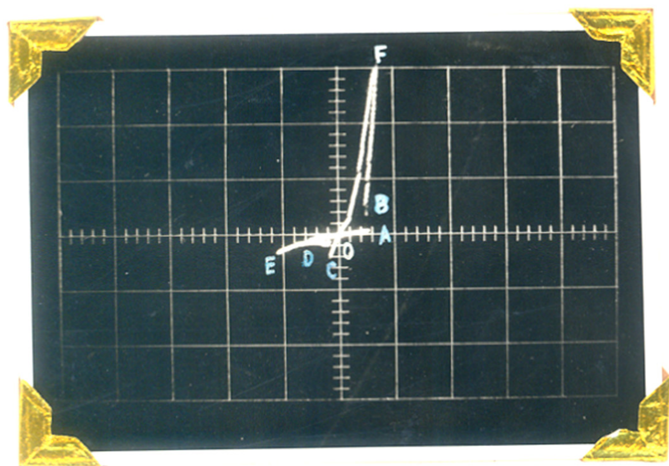


Fig : 21 : Low voltage I-V characteristic of Al-CdS-Au diode in the post-breakdown stage.

X - 4 small divisions = 1 volt. Y - 4 small divisions = 0.25 ma

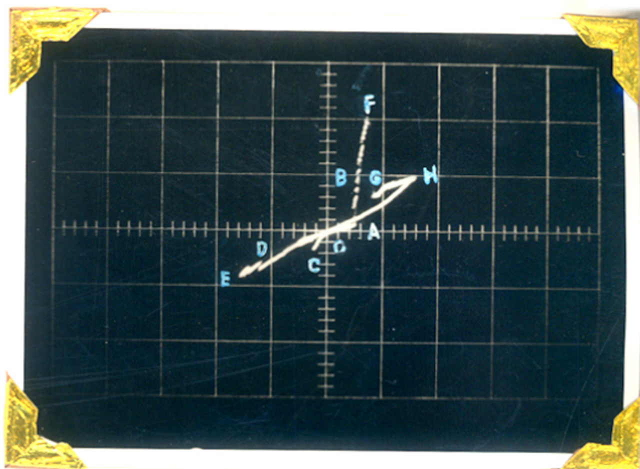


Fig: 22 : High voltage I-V characteristic of Al-CdS-Au diode in the post-breakdown stage.

X - 4 small divisions = 1 volt. Y - 4 small divisions = 0.5 ma

gives poor reproducibility. For the same reason, gold instead of copper is used as the second electrode. In the following paragraphs the behaviour of the Au-CdS-Al and Al-CdS-Au is described.

In the pre-breakdown stage both these sandwiches have properties similar to those of the sandwiches discussed under (1) above, except that in present case the structure shows high resistance only when the gold electrode is made negative irrespective of whether it is at the top or bottom, whereas in the earlier cases the high resistance was observed when the bottom electrode was made negative. Furthermore, the breakdown voltage V_x is somewhat higher than that in Al-CdS-Al structure having approximately the same cadmium sulphide thickness.

In the post-breakdown stage a rather interesting behaviour is observed. The current-voltage curve shows two types of characteristics depending on the amplitude of the applied voltage pulse.

(a) Low voltage range

Figure 21 shows the I-V characteristic for Al-CdS-Au diode in the low voltage range in the post-breakdown stage. Although the dual negative resistance is exhibited as before but the nature of the curve is different which can be described as follows. When the aluminium (bottom electrode in Al-CdS-Au diodes and top electrode in Au-CdS-Al diodes) electrode is negative and the sample is in the low conductivity state (curve OA) a transition from low conductivity takes place, say at A(0.5 to 0.7 volts). This transition is similar to that in Al-CdS-Al giving rise to a current controlled negative resistance region. The only

difference is that the value of V_A is much smaller than that in Al-CdS-Al structure. Secondly, the drop in voltage i.e. $V_A - V_B$ is very small. This can be seen from the steep rise of current from point A to B. When the voltage is decreased from V_B this high conductivity state is maintained till the voltage equal to V_B in the opposite direction is reached (V_C), where the transition from high conductivity state to low conductivity state takes place through a voltage controlled negative resistance region. Here V_D is higher than V_A which was not so, ($V_A \simeq V_D$) in Al-CdS-Al structure. Furthermore, this nature of the curve as a whole is not affected on increasing the frequency of the applied voltage pulse, which is contrary to what was obtained in the Al-CdS-Al structure. Secondly, the peak current in CCNR side is greater than that in the VCNR side whereas it was just the opposite for Al-CdS-Al sandwich diodes.

(b) High voltage

If the voltage is increased further above V_B (after tracing the path OAB and aluminium negative) the path BF is followed (in agreement with the earlier observations on Al-CdS-Al structure). However, at F the system switches from high to low conductivity state through the path FGH (Fig.22). This is different from the Al-CdS-Al system where no such behaviour is observed. After decreasing the voltage from H the curve (i) either

retraces the path HGFBOCDE or (ii) follows a new path HGAOC'DEO. It can be seen that in the first case the behaviour is similar to that described earlier for the low voltage case of Al-CdS-Au in the lower right hand quadrant (VCNR side). When the path HGAOC'DEO is followed the loop GFBO is missed out and VCNR peak is much reduced. Furthermore, this peak goes on reducing on repeated cycling till a stage is reached where no negative resistance (neither CCNR nor VCNR) is observed. If the field is made off for sometime the structure regains the initial negative resistance characteristic.

It is generally observed that if the frequency of cycling is small then the behaviour described under (i) is followed, whereas at higher frequencies that under (ii) is observed. Furthermore, in the Au-CdS-Al diodes a direct shorting is observed in many samples and the behaviour described above is rarely observed.

Both the electrodes are gold (or copper)

In Au-CdS-Au structures initially (i.e. corresponding to the pre-breakdown stage of the earlier samples) we get a symmetrical I-V characteristic and no rectification is observ-ed. When the applied voltage is increased the transformation to the low resistance structure (corresponding to the post-breakdown stage of the earlier cases) is never obtained, even if one has reached the destructive breakdown point of the sample. In some samples direct shorting between two gold

electrodes is observed even with thicker CdS films.

The above study of the effect of the electrode material on the I-V characteristic of metal cadmium sulphide sandwiches leads us to the conclusions that (i) the dual negative resistance is observed only when at least one of the electrodes is aluminium or indium and (ii) for any sample showing dual negative resistance $|V_B| \simeq |V_C|$ but the exact value of V_B or V_C varies from sample to sample depending on the material of the electrodes.

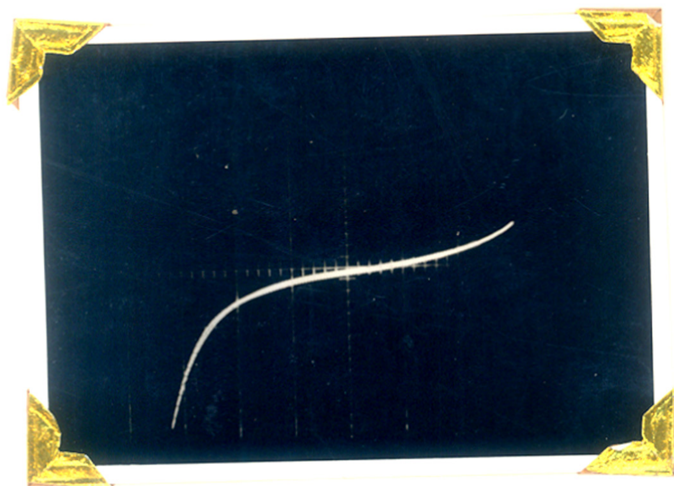


Fig : 23 : I-V characteristic of Al-CdS-Al diode at liquid air temperature in the pre-breakdown stage.

X - 4 small divisions = 2 volt. Y - 4 small divisions = 5   a.

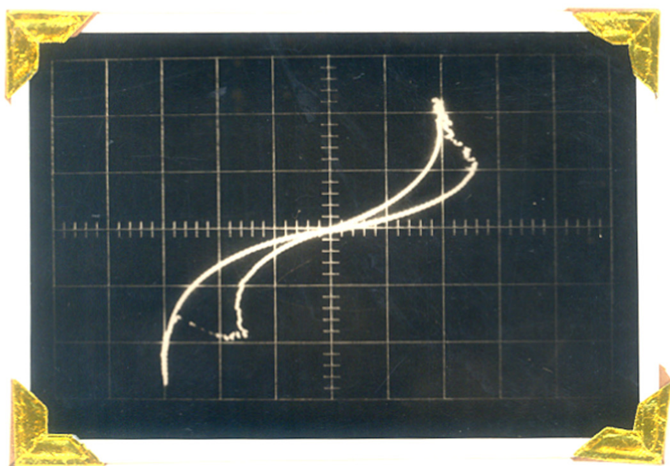


Fig : 24 : I-V characteristic of Al-CdS-Al diode at -170°C in the post-breakdown stage.

X - 4 small divisions = 1 volt. Y = 4 small divisions = 5   ma.

THE EFFECT OF AMBIENT TEMPERATURE

The current-voltage characteristics of Al-CdS-Al structure have also been studied at different temperatures. Al-CdS-Al sandwich structures have been prepared as usual and the I-V characteristics are measured at various temperatures from 77°K to 350°K as described earlier on page 47. Both the pre-breakdown stage as well as the post-breakdown stage with dual negative resistance are observed.

Pre-breakdown stage

In this stage the current at any given voltage, in general, decreases on decreasing the temperature. Fig.23 shows that I-V curve for the sample at liquid air temperature. Secondly, V_x, the voltage required for transformation from pre-breakdown to post-breakdown stage increases on decreasing temperature whereas the hysteresis effect decreases. However, the rectification is not affected.

Post-breakdown stage

Figures 17 and 24 show the I-V curve of Al-CdS-Al at room temperature and at -170°C respectively. It can be seen that the shape of the I-V curve remains unchanged with temperature. However, the values of the critical voltages V_A, V_B, V_C and V_D are, to some extent, affected although no systematic change has been observed. Sometimes the value of V_C decreases and a sudden increase in current at V_C is observed. The current density at any given voltage and the area under the loop, in

general, decreases slowly with decreasing temperature. Table No.7 gives the values of different critical voltages at various temperatures.

Table No.7

Effect of ambient temperature
Thickness of the CdS film : 2.000×10^{-4} cm

Temperature °C	Post-breakdown stage Critical voltages in volts			
	V_A	V_B	V_C	V_D
-170	3.35	2.50	2.45	3.65
-142	3.25	2.50	2.45	3.65
- 97	3.20	2.50	2.45	3.60
- 75	3.15	2.50	1.60	3.50
- 53	3.12	2.40	1.20	3.45
- 32	3.10	2.20	2.10	3.40
- 16	3.05	2.20	2.10	3.30
+ 20	3.05	2.00	2.00	3.25
+ 37	3.10	2.50	2.40	3.40

D) EFFECT OF THICKNESS

The thickness of the cadmium sulphide layer in Al-CdS-Al structure has been varied from 1.0 μ to 2.0 μ by evaporating to completeness different amounts of cadmium sulphide kept in the filament. Other conditions have been maintained identical during all the depositions. The current-voltage characteristics show the following dependence on thickness where the other features remain similar to what has been discussed earlier.

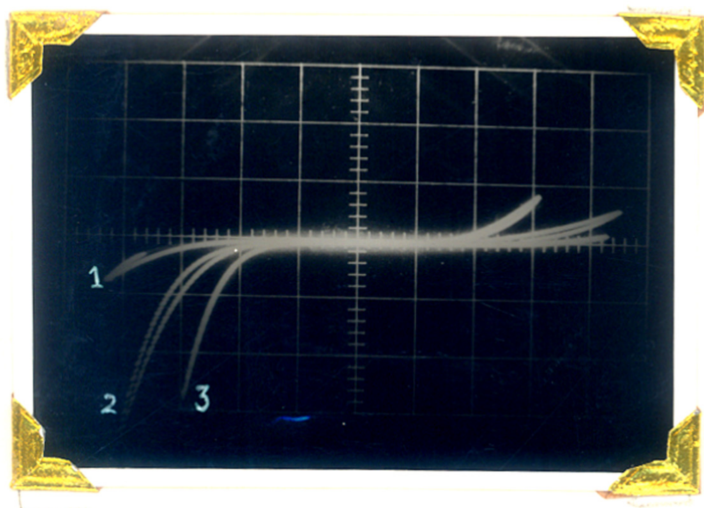


Fig : 25 : Effect of thickness of the I-V characteristic of Al-CdS-Al diode in the pre-breakdown stage.

X - 4 small divisions = 1 volt. Y - 4 small divisions = 5 a.

Pre-breakdown stage

(i) Decrease in current density as the thickness increases, and

(ii) Increase in V_x as the thickness increases.

In Fig. 25 the curves marked (1), (2) and (3) are respectively for the cadmium sulphide thickness in decreasing order. We can see the current density on both the sides decreases as the thickness increases. Furthermore, the recti-fication effect as observed in Fig.15 is reduced in thicker films and the same is also true for the hysteresis effect on the high resistance side. Table No.8 gives the values of V_X for different samples, from where we can see that the breakdown voltage increases with increasing thickness.

Post-breakdown stage

In the post-breakdown stage the dual negative resistance is observed even in thicker films but there is a small increase in the values of critical voltages V_A, V_B, V_C and V_D in these films. However, this increase is less than that in V_X. The effect on the current density is also not so pronounced. Table No.8 summarises these observations.

Table No.8
Effect of thickness

No.	Thickness of CdS x 10^{-4} cm	Breakdown Voltage V_X in volts	Critical voltages in volts			
			V_A	V_B	V_C	V_D
1	1.036	3.50	3.05	2.00	2.05	3.40
2	1.331	4.00	3.05	2.05	2.05	3.45
3	1.687	4.50	3.10	2.05	2.00	3.50
4	2.130	4.75	3.15	2.05	2.05	3.45

E. EFFECT OF SOME OTHER PARAMETERS

In this section we discuss the effect of:

(1) Deposition conditions during cadmium sulphide deposition.

(2) Intermediate exposure to air before or after cadmium sulphide deposition.

(3) Heat treatments of the deposited cadmium sulphide films.

(4) Doping of cadmium sulphide powder before evaporation.

1) Deposition conditions

It has been observed earlier that the nature of the vacuum deposited cadmium sulphide films vary with the deposition conditions[80]. The resistivity of the film depends largely on the amount of excess Cd in the film. For example, cadmium sulphide deposited on a substrate kept at temperatures above 200°C under a pressure greater than 10^{-5} torr is known to give stoichiometric films whereas that deposited at room temperature gives excess cadmium.

The effect of variation in:

(i) Source temperature.

(ii) Vacuum conditions, and

(iii) Substrate temperature on the current voltage characteristics of the Al-CdS-Al has therefore been investigated.

(i) Source temperature :

The source (filament) temperature during the cadmium sulphide deposition has been varied between $800^{\circ}C$ to $1000^{\circ}C$. Above $1000^{\circ}C$ there is too much of spurting. The films are transparent and have a high resistivity in all cases. The variation in filament temperature does not show any appreciable change in the current voltage characteristic of the diodes.

(ii) Vacuum conditions

The samples prepared by depositing cadmium sulphide films at vacuum of the order of 10^{-3} - 10^{-4} torr give very high order of reproducibility and consistant I-V characteristics, while those prepared at 10^{-6} torr or in sulphur atmosphere show a poor reproducibility, although the features remain more or less the same. Furthermore, the value of V_X is larger in samples prepared at 10^{-6} torr(6-7 volts) than in those prepared at pressure of the order of 10^{-3} - 10^{-4} torr(3-5 volts). Amongst the cadmium sulphide samples deposited at a sulphur pressure of 10^{-6} torr, some show initially a pre-breakdown stage as usual which is transformed into an intermediate stage where a dual negative resistance is observed but the polarity for CCNR and VCNR is interchanged i.e. the CCNR region is observed when the top electrode is negative while the VCNR region is observed when the bottom electrode is negative. This intermediate stage is observed till the voltage is below a certain threshold, at which point a second transformation takes place and the structure gives the usual current voltage characteristic as in Fig.17. Further increase in voltage does not change the characteristic. The films deposited at 10^{-6} torr

sometimes show the above mentioned intermediate stage but very rarely.

(iii) substrate temperature

The non-stoichiometry in cadmium sulphide films due to excess cadmium can be removed by depositing cadmium sulphide on hot substrates[80]. This is due to the fact that above 150°C the vapour pressure of cadmium becomes $\simeq 10^{-5}$ torr and the condensing probability (on the substrate above 150°C) for cadmium as well as sulphur becomes nearly equal. The substrate temperature has therefore been varied from room temperature to 150°C and its effect on the I-V characteristics of the diode is studied. The samples are prepared as described on page 42 .

The samples prepared below 100°C show the usual current-voltage characteristics. The voltage at which the pre-breakdown stage transforms to the second stage (i.e. V_X) increases slowly as the substrate temperature increases. For the samples prepared at the substrate temperature of 150°C, the value V_X is observed to be of the order of 10-15 volts. In thin films sometimes the transformation does not occur because they burn away before that. The samples where this transformation is achieved show the dual negative resistance characteristic. Furthermore, the resistivity increases whereas the hysteresis effects and the current rectification in the pre-breakdown stage decrease as the substrate temperature is increased. This can be seen from the fact that the current at any voltage in the pre-breakdown stage is less for samples deposited on substrates kept at higher temperatures. In the post-breakdown stage the values of the critical voltages

V_A, V_B, V_C and V_D remain nearly unaltered. These observations show that the effect of substrate temperature is pronounced on the pre-breakdown stage but not on the post-breakdown stage. Table No.9 lists the values of the different critical voltages for the samples deposited at various substrate temperatures.

Table No.9

Effect of substrate temperature

No.	Substrate temp. ^oC	Thickness of CdS films x 10^{-4} cm.	Breakdown voltage volts (V_x)
1	30	2.130	4.75
2	50	1.500	5.20
3	100	1.1000	6.00
4	150	1.010	10.50

2) Intermediate exposure to air

The observed assymetry in the current-voltage characteristic in the post-breakdown stage including the fact that the CCNR occurs only when the bottom electrode is negative and the VCNR when the top electrode is negative, suggeststhat possibly the two metal-cadmium sulphide contacts may be different in nature. This may be due to the fact that we are exposing the first aluminium film to air before cadmium sulphide is deposited which may give a thin aluminium oxide layer leading to the observed assymetry. Alternatively, it is also possible that a thin

cadmium oxide layer or a layer of adsorbed oxygen or water vapour may be forming on the deposited CdS before the second deposition of Al. The diodes have therefore been prepared after eliminating these intermediate exposures to air and their I-V characteristics have been measured. However, the current voltage characteristics show no appreciable change from the usual behaviour. In the samples prepared without exposing to air before cadmium sulphide deposition, the hysteresis and the rectification are reduced considerably while they are increased in samples in which the exposure is avoided after the deposition of cadmium sulphide. This effect is also increased when the first deposited aluminium is exposed to dry oxygen. In all the samples the post-breakdown behaviour remains unchanged. The field direction required for the CCNR or the VCNR remains unaltered; showing that the assymetry in the structure is not affected by these changes in the ambient conditions during depositions.

3 Heat treatments

It is known that heating cadmium sulphide films in vacuum, in inert atmosphere or in sulphur atmosphere removes excess cadmium and makes the compound stoichiometric[60]. The samples prepared during our investigations have been heated in different atmospheres with a view to see its effect on the I-V characteristic of the diodes.

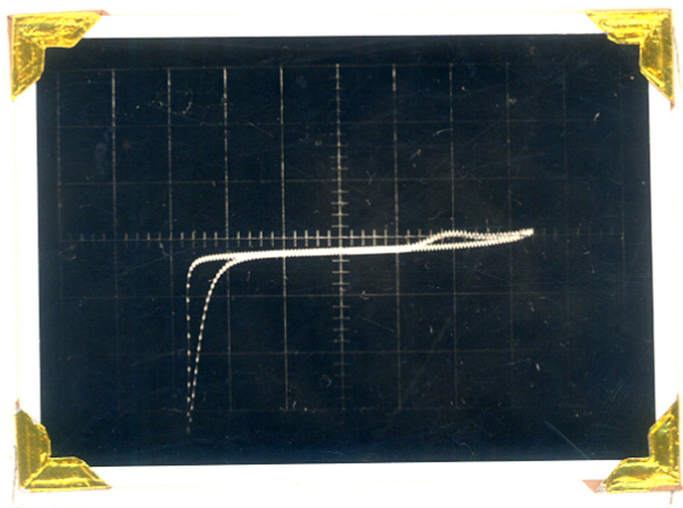


Fig : 26 : I-V characteristic of Al-CdS-Al diode in the pre-breakdown stage. The CdS film is heated in vacuum,

X - 4 small divisions = 1 volt. Y - 4 small divisions = 5 a

(a) Heating in vacuum

For diodes, where the deposited cadmium sulphide film has been heated in vacuum, the transformation from the pre-breakdown to post-breakdown stage often takes place in two steps. The first step occurs at about 3.75 volts and the second is observed at about 7.5 volts. After this second breakdown the structure shows the usual dual negative resistance characteristic. Before the first breakdown takes place a small peak in current on the high resistance side is sometimes observed (Fig.26), which vanishes on repeated cycling. In the dual negative resistance stage the values of the critical voltages V_A, V_B, V_C and V_D are increased to a smaller extent as compared to the samples in which the cadmium sulphide film has not been heated. Furthermore, during the transition from high conductivity state to the low conductivity state (point C) the decrease in current is not so pronounced.

(b) Heating in sulphur atmosphere

Current-voltage characteristics similar to that described above are exhibited. However, in these structures the above-mentioned current peak on the high resistance side of the pre-breakdown stage is not observed. Furthermore, in the post-breakdown stage the values of the critical voltages are increased as compared to unheated samples but only slightly.

Doping of the cadmium sulphide

With a view to examine the role of donor or acceptor levels in the observed I-V characteristics, samples containing CdS doped with In_2S_3 and Ag_2S have been prepared and the current voltage characteristics are studied.

In the diodes having cadmium sulphide doped with impurities the transformation voltage V_X at which the pre-breakdown stage goes to the post-breakdown stage slowly decreases with the increase in the concentration of In_2S_3. No other significant change from the usual pattern is observed. Sometimes, the transition from the low conductivity state to high conductivity state takes place at a slightly lower voltage (V_A) and the increase in the current is much steeper as compared to the undoped samples. This effect is more pronounced in samples having high concentrations of In_2S_3. The other critical voltages remain more or less unaffected.

Similar characteristic features are observed in the diodes containing Ag_2S doped cadmium sulphide. The value of V_X is more in these diodes than in those containing In_2S_3 doped cadmium sulphide. However, in this case the V_X is more or less independent of the Ag_2S concentration.

Table No.10

Effect of doping

Thickness of the CdS film 2.5×10^{-4} cms.

No.	Sample	V_X	V_A	V_B	V_C	V_D
1	N 1	5.00	3.20	2.40	2.35	3.40
2	N 2	4.50	3.20	2.40	2.40	3.40
3	N 3	4.50	3.15	2.45	2.40	3.35
4	N 4	3.25	3.10	2.35	2.35	3.35
5	P 1	7.50	3.35	2.45	2.40	3.50
6	P 2	7.55	3.40	2.40	2.40	3.50
7	P 3	7.50	3.45	2.35	2.35	3.45
8	P 4	7.45	3.40	2.35	2.40	3.55

CHAPTER - IV

D I S C U S S I O N

CHAPTER - IV

D I S C U S S I O N

The phenomenon of dual negative resistance observed during the study of the current-voltage characteristics of metal-cadmium sulphide-metal thin film sandwich structures has the following features.

(1) The behaviour is characterised by two distinct stages. In the first or pre-breakdown stage, the structure has a high resistance. After a critical field is applied the structure goes irreversibly into a second stage where it has an overall low resistance and where the dual negative resistance phenomenon is observed.

(2) In the post-breakdown stage, when the negative voltage on the bottom electrode is increased, the curve follows a low conductivity path upto a critical voltage, at which point the structure transforms into a high conductivity state through a current controlled negative resistance (CCNR) region. On decreasing the voltage the high conductivity state is maintained till a critical voltage in opposite direction is reached, where the structure switches back to the low conductivity state through a voltage controlled negative resistance (VCNR) region.

(3) The phenomenon is observed if the electrodes are either aluminium or indium.

(4) If both the electrodes are gold (or copper), then this property of dual negative resistance disappears.

(5) However, if one electrode is gold and the other is aluminium, the dual negative resistance (DNR) is observed with some modifications.

(6) The nature of variations in the current-voltage curve due to changes in the nature of the electrodes, cadmium sulphide film thickness, ambient temperature, impurity in cadmium sulphide, heat and surface treatments on cadmium sulphide film, etc. shows that the conduction in the pre-breakdown stage is governed by bulk of cadmium sulphide while that in the post-breakdown stage is governed mainly by metal-cadmium sulphide contact.

In general, any mechanism for the observed characteristic must explain:

(i) Pre-breakdown high resistance stage,

(ii) Forming and irreversible breakdown, and

(iii) Dual negative resistance in the post-breakdown stage.

In the following sections a possible explanation for the above characteristic is given.

A) PRE-BREAKDOWN STAGE

We first examine the possibility of space-charge-limited current in the pre-breakdown stage because such currents have already been reported through single crystals of cadmium sulphide[15] and cadmium sulphide films[16] (deposited in vacuum) and also the metals aluminium and indium give Ohmic contacts[82] to these films which facilitate SCL current.

Mott and Gurney[11] and Rose[13] have derived an equation for such currents in a perfect insulator (see Table No. 1). However, the observed values of current densities are usually much lower, because in practice, the insulator contains a large number of traps which trap the injected carriers and thus lower the current. Apart from these traps, the insulator does have some free carriers in conduction band in thermal equilibrium with the shallow trap levels and donor levels (n-type cadmium sulphide). In the presence of such imperfections, the equation for the space charge limited currents gets modified (see Table No.1).

At low voltages i.e. when $n_o > n$, the conduction is governed by "n_o" and the current is given by the well-known Ohm's Law. At higher voltages the injected carrier density becomes large as compared to "n_o" and therefore the space charge limited law is observed. This behaviour on log-log plot of I-V curve gives a straight line of slope = 1 (corresponding to Ohm's Law) at lower voltage; and at higher voltage i.e. when the SCL law is obeyed, the slope changes to two.

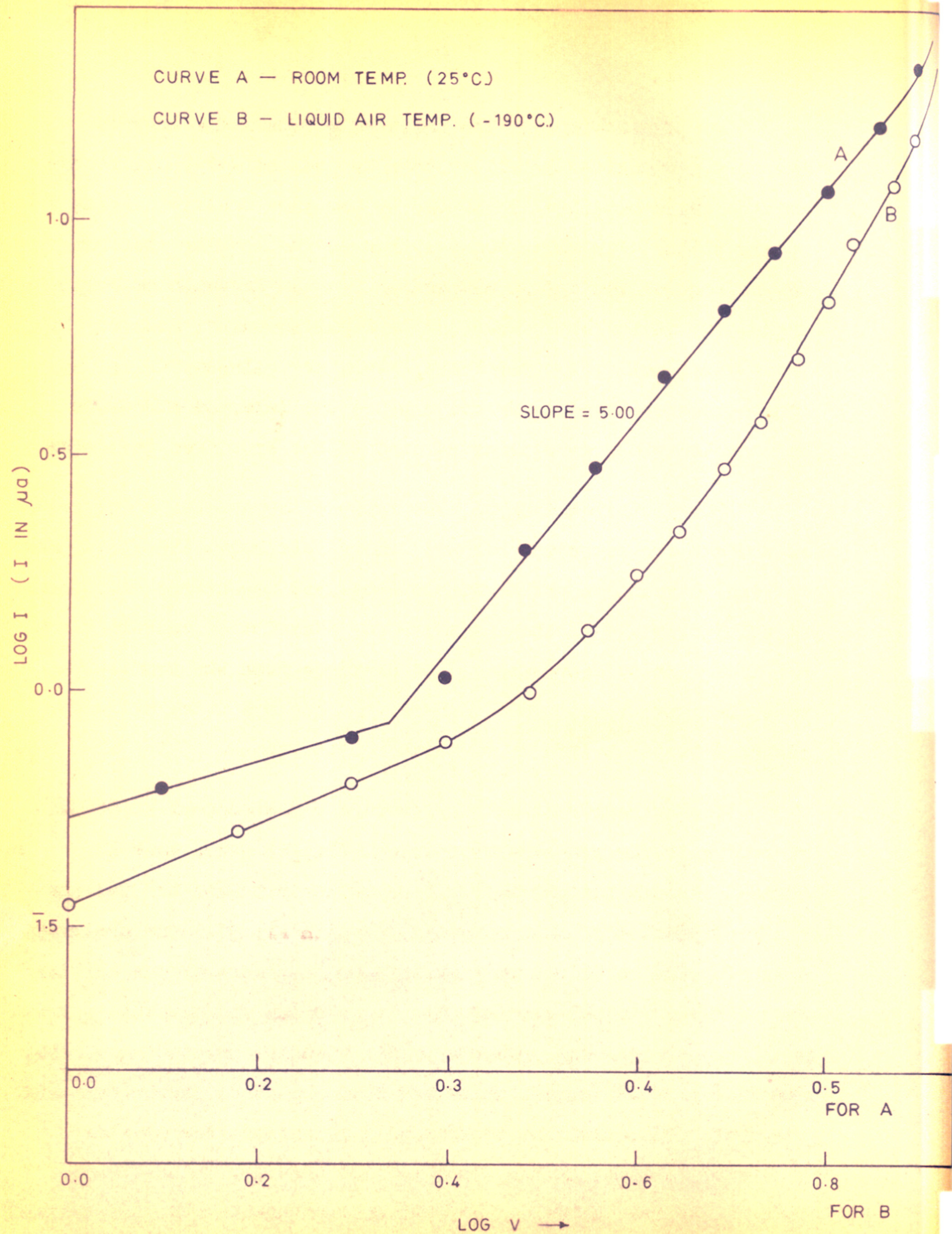


FIG. 27. PLOT OF LOG I V/S LOG V FOR PRE BREAKDOWN STAGE

For shallow traps, the injected carriers are trapped and only a fraction ($\theta < 1$) of them is available for conduction and the drift mobility is reduced by the same fraction giving a straight line with slope equal to two on the log-log plot but the current is reduced by a fraction 'θ'. In presence of deep traps, 'θ' in the above equation is equal to unity, because the traps being well below the Fermi level, are already filled up at room temperature and do not capture the injected electrons and the behaviour is similar to that of the trap free insulator.

For distributed traps, two types of dependence of current on voltage are reported. For uniformly distributed traps Rose[13] has derived an equation which gives exponential dependence of current on voltage, while if the traps are not distributed uniformly but the trap-density decreases as the distance from the conduction band increases, then $I \propto V^n$, where ($n > 1$). The value of n is governed by the nature of the trap distribution.

The current voltage characteristic of Al-CdS-Al sandwich structure in the pre-breakdown stage (Fig.15) shows that the current through the sample varies non-linearly with the voltage. The log-log plot of this curve is shown in Fig.27. The observed nature of the curve can be explained on the basis of one carrier space-charge-limited-current flow in presence of thermally generated free carriers and presence of distributed shallow traps. The first part of the curve, which has slope equal to one, represents the Ohmic conduction due to thermally generated free carriers. At higher voltages the injected carrier density, which exceeds that of the free carriers, governs the conduction and gives rise

to the space-charge-limited law. The slope for the pure SCL law should be equal to two. However, in the figure we see that the slope is $\simeq 5$. This is in agreement with the deduction of Rose[13] who predicted a high power dependence when the traps are not distributed uniformly, but the trap density decreases, as the depth from the conduction band increases.

The pulse measurement[89] on such structures has shown higher current value than that observed in the above experiments. This points towards the presence of shallow traps. The hysteresis in the pre-breakdown stage in both the directions can be attributed to these traps. These traps can be of two types, namely, fast and slow. The former capture and release the carriers rapidly, while the latter, do so slowly. The hysteresis can be explained as due to the presence of the slow traps. The decrease in current density, on keeping the voltage for some time and also on repeated cycling, is due to these slow traps. Similar observations of decrease in current on standing has been reported by Smith and Rose[15] in single crystal cadmium sulphide. It is also possible that these slow states (traps) are at the surface. Such states are suggested by Bardeen[90]. Sometimes the carriers are trapped permanently and their restoration to original state is difficult.

The increased hysteresis and resistance when the bottom electrode (Al) is made negative are likely to be due to a thin oxide film on this electrode. This oxide film offers an extra barrier for injection from the lower electrode to CdS but not in the reverse direction. Hysteresis and rectification are reduced in the samples prepared without exposing them to air prior to

cadmium sulphide deposition; while they are increased in the samples where the bottom electrode (Al) is deliberately exposed to dry oxygen.

The adsorbed layer of oxygen or water vapour[91] on the deposited cadmium sulphide gives rise to the surface states which may also contribute to the above assymetry in the I-V curve. The absence of pronounced rectification in Al-CdS-Au diodes can be accounted for as due to such surface states which mask the work function difference between the metals.

These effects, however, can also be attributed to possible non-stoichiometry in the cadmium sulphide film due to a high resistive layer near the bottom electrode (Al).

The results of the effect of variations in the temperature of the sample on the I-V characteristic in the pre-breakdown stage support the presence of traps and thermally generated free carriers. The decrease in temperature gives rise to decreased number of thermally generated free carriers, hence the total current decreases (Fig.27).

The increase in cadmium sulphide thickness decreases the current density at any voltage. This dependence clearly indicates that the conduction is mainly governed by the bulk of cadmium sulphide. The field dependence rather than the voltage dependence of the V_X confirms this.

Electronic tunneling is one of the other mechanisms suggested for the electron transport through thin insulating films. Earlier calculations and experimental results[7] have shown that the

tunneling current increases exponentially at high voltages while at low voltages ($V < \phi_{met}$) the Ohmic behaviour is followed. The main feature of this process is that the current is independent of temperature[25]. For our samples the plot of log I vs voltage has shown the initial Ohmic behaviour, but at higher voltages large departure from the exponential behaviour is observed. Secondly, the tunneling probability decreases exponentially as the thickness of the insulating film increases. The probability becomes very small for films greater than 100Å. Our cadmium sulphide film thickness is estimated to be 0.5 - 2.0 μ and hence the tunneling probability is negligible. Furthermore, the Al-CdS contact can be treated as an Ohmic contact and therefore tunneling is ruled out.

Schottky field emission[25] also does not appear to be applicable. The current-voltage relation for this type of conduction should give a straight line on the plot of log I vs $V^{1/2}$. Recent calculations have, however, suggested that the log I vs $V^{1/4}$ plot should be straight line. Our samples do not show such dependence. Secondly, this type of conduction should be strongly temperature dependent and that the log I/T^2 vs $1/T$ plot should give a straight line, if this type of conduction is predominant. Our samples show very poor agreement with such a behaviour. Further, it has been shown that in case of Schottky field emission the capacity 'C' of sample is proportional

to $\sqrt{1/V}$ where V is the applied voltage. Recent measurements done by Srivastava[89] in this laboratory on such diodes do not show such a dependence. In view of all these factors, the possibility of the Schottky field emission in our diodes can also be ruled out.

Other mechanisms such as impurity field emission, space charge limited tunnel emission, avalanche breakdown, Zener breakdown, etc. have been examined and ruled out on the basis of experimental results. It is, therefore, concluded that the conduction in the prebreakdown stage, in Al-CdS-Al structure, is space-charge-limited.

B IRREVERSIBLE TRANSFORMATION (BREAKDOWN)

The initial high resistance (pre-breakdown) stage, described on page 50 transforms irreversibly to the post-breakdown stage where the sample shows an overall low resistance. This transformation takes place at a voltage V_X, which depends on various factors as summarized below:

(1) If the thickness of the cadmium sulphide increases, V_X increases.

(2) If the ambient temperature of the sample decreases, V_X increases.

(3) Doping of the cadmium sulphide powder, before depositing by In_2S_3 decreases V_X, while doping by Ag_2S increases V_X.

(4) The increase in substrate temperature during cadmium sulphide deposition increases V_X and if temperatures above 150°C are used sometimes films burn away, before this irreversible transformation.

(5) This irreversible breakdown can be achieved by applying the voltage in either direction.

(6) The presence of aluminium or indium seems to be essential, as no breakdown is observed when both the electrodes are gold or copper.

The thickness dependence of V_X clearly shows that the breakdown leading to the conductivity development is a bulk phenomenon. As the thickness increases the transformation voltage V_X increases which shows that the electrical field rather than the

voltage governs the breakdown. The effect of the temperature also supports this conclusion. Decrease in sample temperature decreases the number of free carriers, so higher voltages have to be applied to attain the required carrier density. These observations are similar to that reported for avalanche breakdown in Au-CdS-Au diodes by Chopra[43]. Furthermore, the doping with Ag_2S gives higher values of V_X, because it decreases the free carriers in the sample in the pre-breakdown stage. The addition of In_2S_3 on the other hand, increases the free carriers in cadmium sulphide and hence V_X decreases.

The effect of substrate temperature on V_X is quite significant. It has been explained earlier that the cadmium sulphide films deposited on hot substrates have higher resistance which is due to the decrease in excess cadmium concentration. Thus we can conclude that decrease in ~~impurity~~ Cd concentration increases V_X. Similar results are described by Hickmott[63] for the conductivity establishment in metal-oxide-metal diodes. He has suggested that if the oxide impurity concentration is low, high fields are necessary to establish the conductivity. If the impurity concentration is too low, dielectric breakdown occurs before forming of conductivity. Thus the impurities in the insulator are important for this irreversible transformation.

To explain the increased conductivity of single crystals of cadmium sulphide, after application of high fields, Kroger et.al.[77] have suggested the existence of an insulating barrier or a surface layer, which breaks down irreversibly at a critical voltage. Most of the applied voltage drops down across this high resistive layer.

However, our experimental observations do not fit in with this explanation; as the presence of a surface layer does not explain the observed thickness dependence of V_X, as well as the above mentioned impurity effect.

Geller's[59] suggestion of the reduction in the work function at the metal-insulator junction, which increases the metal to insulator electron transfer, as being responsible for the increased conduction in alkali halide crystals containing F centres, also appears unlikely to hold for our present case. Pollack[28] has also suggested a similar forming process in Al-Al_2O_3- Pb diodes due to the establishment of positive space-charge near the negative electrode. Excess aluminium atoms which will act as donors are proposed by Fisher and Giever[7] to explain some of the semiconducting properties, observed in tunnel diodes of Al-Al_2O_3 - Al. Hickmott[57,60] has also suggested a similar forming process to explain the establishment of conductivity in Al-Al_2O_3 - Al diodes. He has proposed a dipole forming of neutral impurities near cathode, the positive end of which lies in the insulating oxide.

The common feature of all these explanations is the establishment of a positive space charge near the cathode. However, many of our observations on the present system cannot be explained by these models. For example, the forming as reported by Pollack[28] is slow and not field dependent and in each cycle the conductivity increases. In our samples the establishment of conductivity takes place at a fixed voltage and it is fast. Secondly, if an ionic

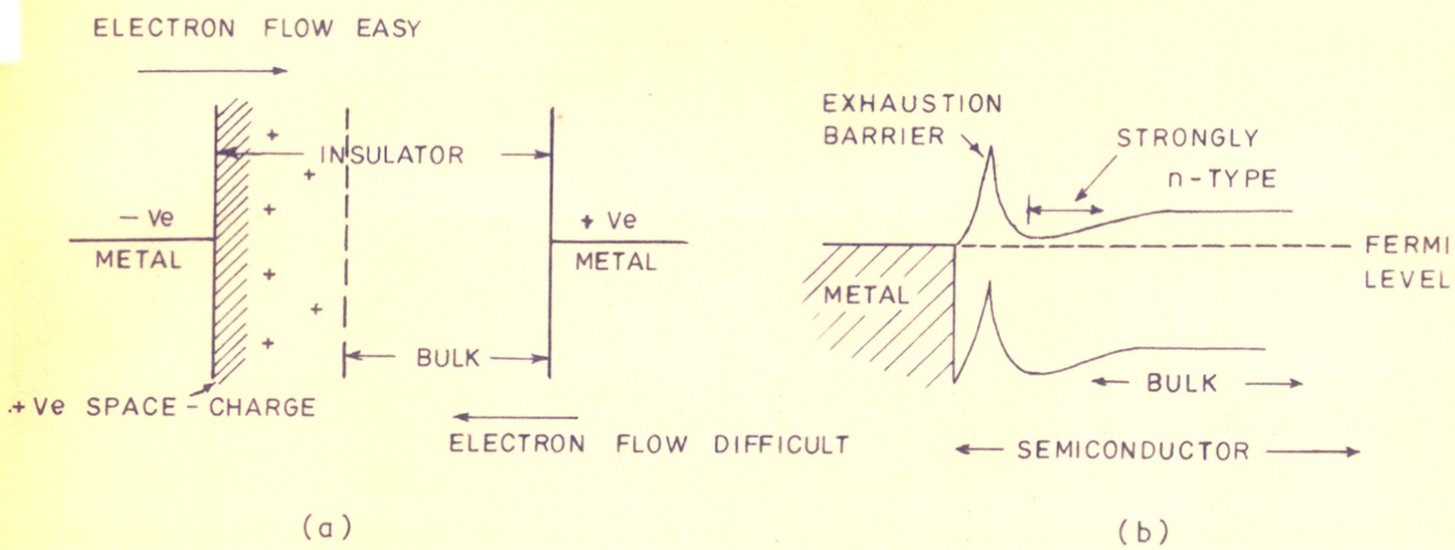


FIG. 28. SCHEMATIC MODEL FOR IRRIVERSIBLE BREAK DOWN

(a) GELLER'S MODEL

(b) KROGER'S MODEL

space-charge-layer is present, then it can drift only slowly and if the polarity is changed quickly after the formation, the space-charge-layer will still be near to the previous cathode and hence the structure will show a rectification. This will be clear from the Figure No.28(a). When the left-hand electrode is negative the current flow will be easy. However, if the polarity is reversed quickly and a positive voltage is applied to this electrode, the positive space-charge-layer will still be near to this electrode and it will oppose the flow of electrons to the anode. So we should observe a rectification which should decrease as the space-charge-layer drifts towards the new cathode. No such behaviour is observed in our samples. On the other hand, the sample remains permanently in the low resistance stage, independent of such polarity changes.

Another possible explanation has been suggested by Hickmott[63] on the basis of an impurity band formation in the bulk of the insulator near the middle of the forbidden energy gap. This band formation takes place due to the field ionization of neutral impurity centres, uniformly distributed throughout the insulator. At a critical field, the ionization becomes large giving rise to two possible changes (i) these ionized impurities form a band and (ii) the metal-oxide potential barrier is reduced,so that the electron passes easily from metal into the insulator. The carriers are electrons injected from metal, but the conduction is governed by the hopping from impurity site to impurity site through the impurity band.

Boer et.al.[93] (1952) have reported a thermal and field breakdown in single crystals of cadmium sulphide. As the applied field increases, the carrier temperature increases giving rise to increased number of carriers. At higher field thermal-electric instability developes creating a conductivity channel through a breakdown. This produces changes in the conductivity of the bulk, partly reversible and partly irreversible. Diemer[94](1954) has explained this as a phenomenon similar to Townsend process in gas discharge. When large currents start flowing, thermal breakdown takes place. Woods[95] (1956) has observed similar irreversible breakdown in single crystals of cadmium sulphide. He has observed increased photoresponse and electrical conductivity after this breakdown occurs. He has suggested that these irreversible changes are bulk changes and furthermore he has ruled out any surface changes or contact phenomena. He has proposed some donor level formation in the bulk. The effect of these donors is similar to that of aluminium or chlorine impurities but no direct correlation has been established.

Our experimental observations are more in agreement with the explanations given by Hickmott, Woods and others, in which the irreversible breakdown and establishment of conductivity is due to a bulk phenomenon rather than due to any change in the nature of contact or breakdown of an insulating layer as suggested by Kroger et.al.[77]. Secondly, the effects of impurity addition, substrate temperature, etc. change the nature of the bulk and hence they affect the pre-breakdown stage. However, they have no effect on the post-breakdown stage.

Two possible suggestions can be given to explain these changes in the bulk of cadmium sulphide viz. (i) removal of traps, (ii) creation of new donor states by diffusion of atoms from electrode into the bulk. In the following paragraphs these possibilities are discussed in some detail.

The presence of traps is supported by the observations such as hysteresis effects and frequency dependence of current-voltage characteristic in the pre-breakdown stage. The decrease in current density on repeated cycling and the observed current-voltage dependence also indicate the presente of traps. However, the exact nature of the traps is not clear at present. They might be due to some chemical impurities or crystal defects such as grain boundaries, dislocations, surface states, point defects etc. These traps decrease the free carriers in the conduction band and thus the conductivity is reduced to a great extent. On decreasing these traps, the carriers in the conduction band increase leading to an increased conductivity. It is possible that this process takes place at a critical field. For example, at higher current densities the temperature of bulk increases and this increase in temperature may remove the traps arising due to grain boundaries. Alternatively, the non-equilibrium charged point defects can get annihilated during migration under the electric field. These changes obviously are non-reversible so that the change from pre- to post-breakdown stage is permanent.

The second possible explanation for increased conductivity is the creation of new donor states by the diffusion of Al in cadmium sulphide. This type of diffusion also modifies the

potential barrier which gives increased efficiency in injection of carriers. The combined effect is to increase the observed conductivity and this change is permanent. Kroger[92] et.al. have suggested a model for such diffused Ohmic contacts (Fig.28 b).

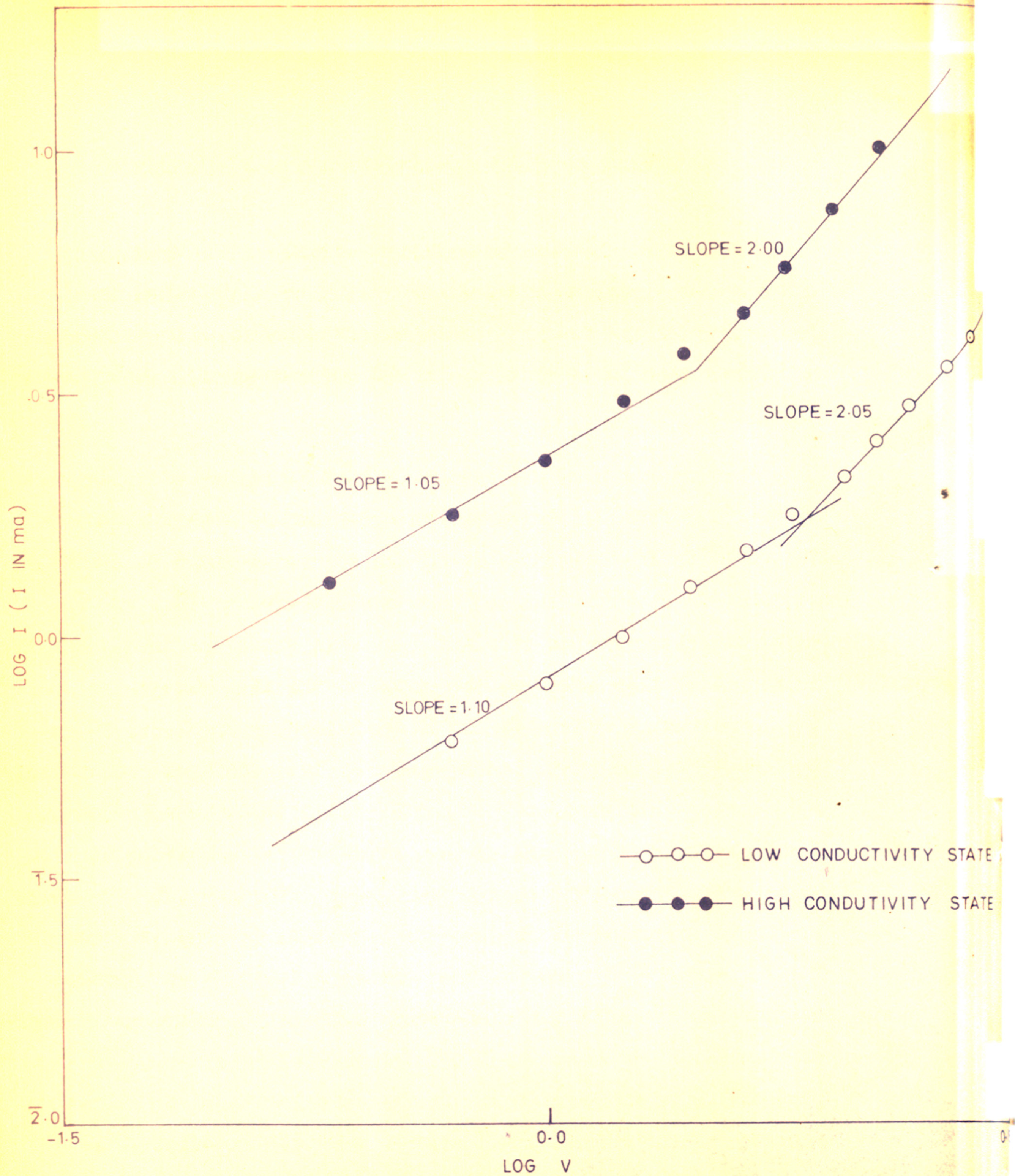


FIG. 29. PLOT OF LOG I V/S LOG V FOR POST-BREAKDOWN STAGE

(c) POST BREAKDOWN STAGE AND DUAL NEGATIVE RESISTANCE

After the above-mentioned irreversible transformation the structure goes to the post-breakdown stage in which the resistance of the sample decreases. This stage is characterised by a dual negative resistance in the current-voltage characteristic (Fig.17).

We can see from the figure 17 that at higher voltages the current in both the stages varies non-linearly with voltage. Fig.29 shows the log-log plot of the current-voltage curve of Fig.17. In both the low and high conductivity states, at low voltages, the curve is straight line with the slope equal to unity and at high voltages, the slope of the line changes to two. The behaviour in figure 29 can be explained on the basis of space-charge-limited currents, in presence of free carriers, in thermal equilibrium with traps. This model will give Ohmic behaviour at low voltages ($n < n_o$) and space-charge-limited behaviour at high voltages ($n > n_o$). The change from low to high conductivity could be due to increased donor sites or reduction of traps present in the low conductivity state. The increased donor sites increase the free carriers in the conduction band and therefore the transition voltage, at which the Ohm's Law changes to space-charge-limited law, should increase. On the other hand, if the traps are removed then this transition voltage would be expected to be constant or shift towards lower value. This transition voltage in high conductivity state is smaller than or equal to the transition voltage in the low conductivity state. This shows

that the high conductivity state is probably due to a process in which the effective trapping is reduced.

The effect of thickness on the critical voltage is negligible atleast for V_B and V_C though a slight increase in V_A and V_D is observed in thicker films. However, this increase is very small as compared with that in the pre-breakdown stage on V_X. The effect of thickness on current density is not pronounced, though slight decrease is observed with thicker films. The current density, in general, decreases slightly as the ambient temperature of the sample is decreased. The substrate heating markedly affects the pre-breakdown stage, but not the dual negative resistance characteristics, once the irreversible breakdown is achieved. From all these observations, one can conclude that in the pre-breakdown stage the properties are field dependent and are controlled by the bulk of cadmium sulphide while those in the post-breakdown stage are voltage-dependent and the bulk has a very small effect on the I-V curve and on the critical voltages.

The effect of electrode materials seems to be one of the important factors in the breakdown and establishment of the dual negative resistance. In Al-CdS-Al structure theCCNR region appears when the bottom electrode is made negative. In Au-CdS-Al and Al-CdS-Au structures the CCNR region appears when Al is made negative. This shows that the presence of aluminium is necessary.

Both the current controlled as well as voltage controlled negative resistances are reported in the literature but no observations similar to dual negative resistance have been reported so far. A hysteresis in I-V curve has been reported by Nicoll[96]

(1958) in CdSe and Bube[97] (1960) in CdS but not the dual negative resistance. The mechanisms suggested to explain the negative resistance are therefore of two types, one for CCNR and the other for VCNR. In the following paragraphs these suggested mechanisms are summarized.

The current controlled negative resistance in bulk has been explained by avalanche injection[40,44], double injection with increase in hole life time[12], avalanche breakdown double injection[46], etc.

In these mechanisms the cause for the transformation of low to high conductivity state is field dependent. When the applied field is reduced lower than that required to maintain the avalanche or to keep the space-charge region stable, the avalanche stops as well as the region gets destroyed and we come to low conductivity state through a CCNR. This gives high reversibility and symmetry in the characteristics. However, in our samples the return to the low conductivity state takes place at a field in reverse direction only and hence the above mechanisms are not appropriate.

Lampert's model[12], based on a dynamic equilibrium between the injected holes and the trapped holes, where at high fields hole trapping is reduced and at low fields it is increased, does not seem to be applicable to the present case because this would lead to a reversible CCNR.

The voltage controlled negative resistance has been suggested to be due to transfer of electrons into sub-bands or levels, situated higher in the energy scale, in the conduction band[48,49,50]. There is a dynamic equilibrium between the electrons in the lower band and that in the upper band and hence the VCNR will be reversible which is contrary to the present observation. The mechanisms based on (i) the electron tunneling through an impurity barrier and increased capture cross-section for repulsive centres at higher fields[51,53], (ii) impurity band formation in the bulk of semiconductor[63], and (iii) space charge layer formation[58], have been examined but they do not explain our observation.

A possible explanation on the basis of domain formation has also been considered. Following Ridley[48] one can assume that current filaments are formed at V_A leading to a CCNR region. These filaments remain stable when the voltage is decreased and change over to field domains at V_C leading to VCNR. The field domains also remain stable when the voltage swing is reversed till one reaches V_A.

It may not be necessary to postulate the formation of both types of domains because even one type of domain can explain the observation. For example, the current filaments in the high conductivity state and filament free CdS in the low conductivity state with a switch over from the former to later at V_C and vice versa at V_A will also explain the result. Alternatively, voltage domains in low conductivity state and domain free CdS in high conductivity is also possible.

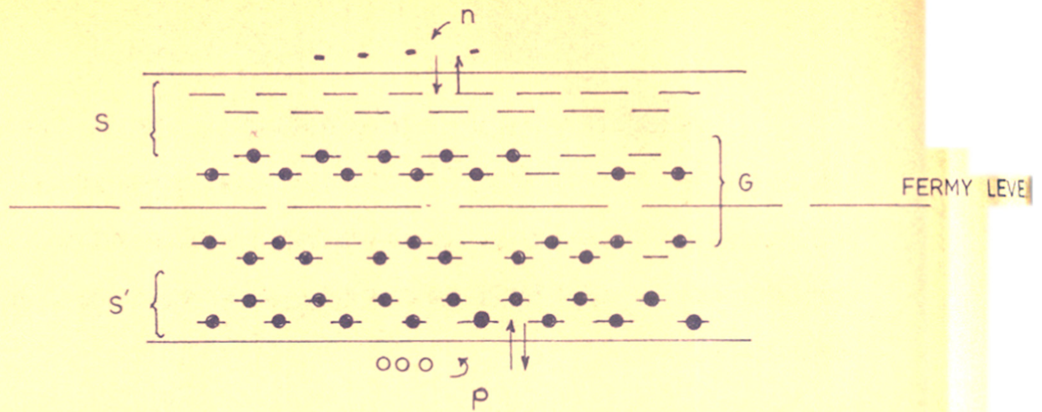
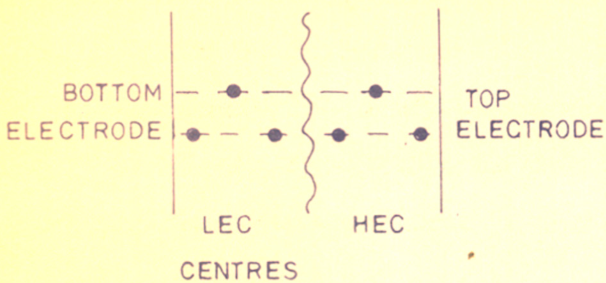
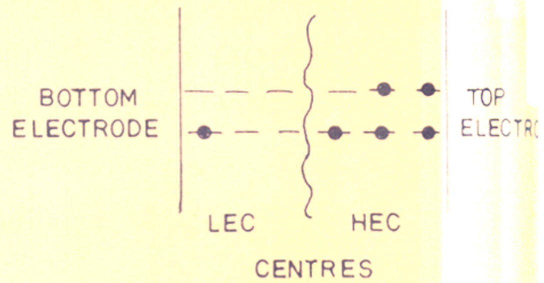


FIG. 30 a. SCHEMATIC MODEL FOR PHOTOCONDUCTOR WITH DISCREET STATES





B) LOW CONDUCTIVITY STATE

C) HIGH CONDUCTIVITY STATE

FIG. 30(b),(c) SCHEMATIC MODEL FOR DNR

Another plausible explanation is the one based on the presence of two classes[98] of trapping centres in the cadmium sulphide. Before we go on to discuss this model we give a brief idea of the nature and the role of traps in cadmium sulphide.

The free carrier density in a semiconductor can be increased by irradiation with photons or high energy radiations or by injecting extra carriers in the respective bands with the help of suitable injecting contacts. The discrete states in the forbidden gap play an important role in the generation and recombination of these carriers. These discrete states are due to the defects in the crystal. The recombination behaviour of the free carriers is not the same at these different states, which are accordingly classified as electron traps, hole traps, deep (ground) and shallow traps; donors, acceptors and recombination centres.

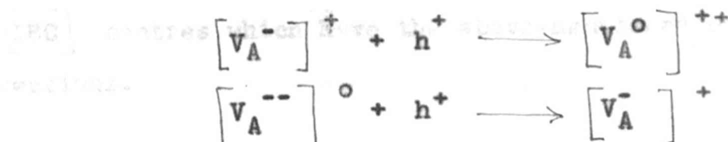
Figure 30(a) gives a schematic model of a photoconductor with different discrete states. The states 'S' near the conduction band are such that the electrons falling into them are re-excited thermally, back into the conduction band and thus are in equilibrium with free electrons in conduction band. Similar states (S') for free holes in the valence band are located near the valence band and are in thermal equilibrium with free holes. Such types of states (S,S') are called as shallow traps. It can be visualised that for the electrons falling into the deep traps the thermal re-excitation is very

difficult and the carriers remain 'trapped' with the states for a very long time. These deep lying states are called ground states. The occupancy of the shallow trap is governed by the thermal equilibrium, while that of the ground states is governed only by the kinetic process of recombinations and hence are called as recombination centres.

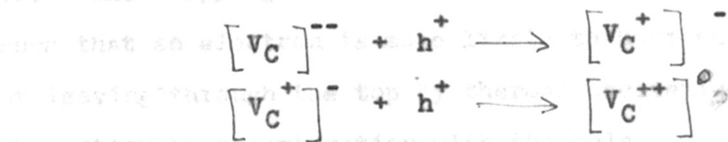
These states have different capture cross-sections for electrons as well as holes. Values in the range 10^{-13} cm^2. to 10^{-22} cm^2. have been reported[99] for the capture cross section in CdS photoconductors. These small values arise from selection rules and from potential barriers surrounding the trapping centres - that is a repulsive coulomb field. Any given centre is likely to have different capture cross sections for electrons and holes.

Cadmium sulphide is known[97,100] to have two classes of ground state trapping centres. The Class I states are described as having high electron capture cross section [HEC] of the order of 10^{-15} cm^2. and it is nearly the same for holes. Class II states can be described as having low electron capture cross section [LEC] of the order of 10^{-20} cm^2. and for holes the capture cross section is of the order of 10^{-15} cm^2. Furthermore, holes falling into [LEC] centres become 'trapped' because they do not capture electrons readily. Crystal defects that have capture cross section properties stipulated above can easily be visualised purely on electrostatic grounds[97].

[HEC] centres



LEC centres



where V_C represents a cation vacancy and V_A an anion vacancy. The sign inside the bracket represents the effective charge of the defect with respect to the crystal.

Kroger *et.al.*[77] have concluded on the basis of conductivity study that the probable height of the anion vacancy with one trapped electron ([HEC] centres) is about 1.8 electron volts above the filled band and that for the cation vacancy with a trapped hole ([LEC] centres) is about 1.3 e.v. above the valence band. According to Bube[97] the infrared quenching phenomena gives the value for [LEC] centres, equal to 1.1 to 1.2 e.v. It can be further added that filling up of [HEC] centres will decrease the electron trapping, as the traps having greater capture cross sections for electrons are decreased, while the emptying of [LEC] centres will not affect the trapping with respect to electrons as the capture cross section is very small.

We now give a brief out line of the phenomenon-logical model, proposed to explain the observed dual negative resistance. Following Rose[98] we make the following postulates:

(1) Our CdS film contains both the [HEC] centres and [LEC] centres which have the above-mentioned capture cross sections.

(2) They are non-interacting under normal conditions.

(3) The trapping factor is purely statistical condition such that an electron is more likely to have an opportunity of leaving through the top by thermal excitation than through the bottom by recombination with the hole.

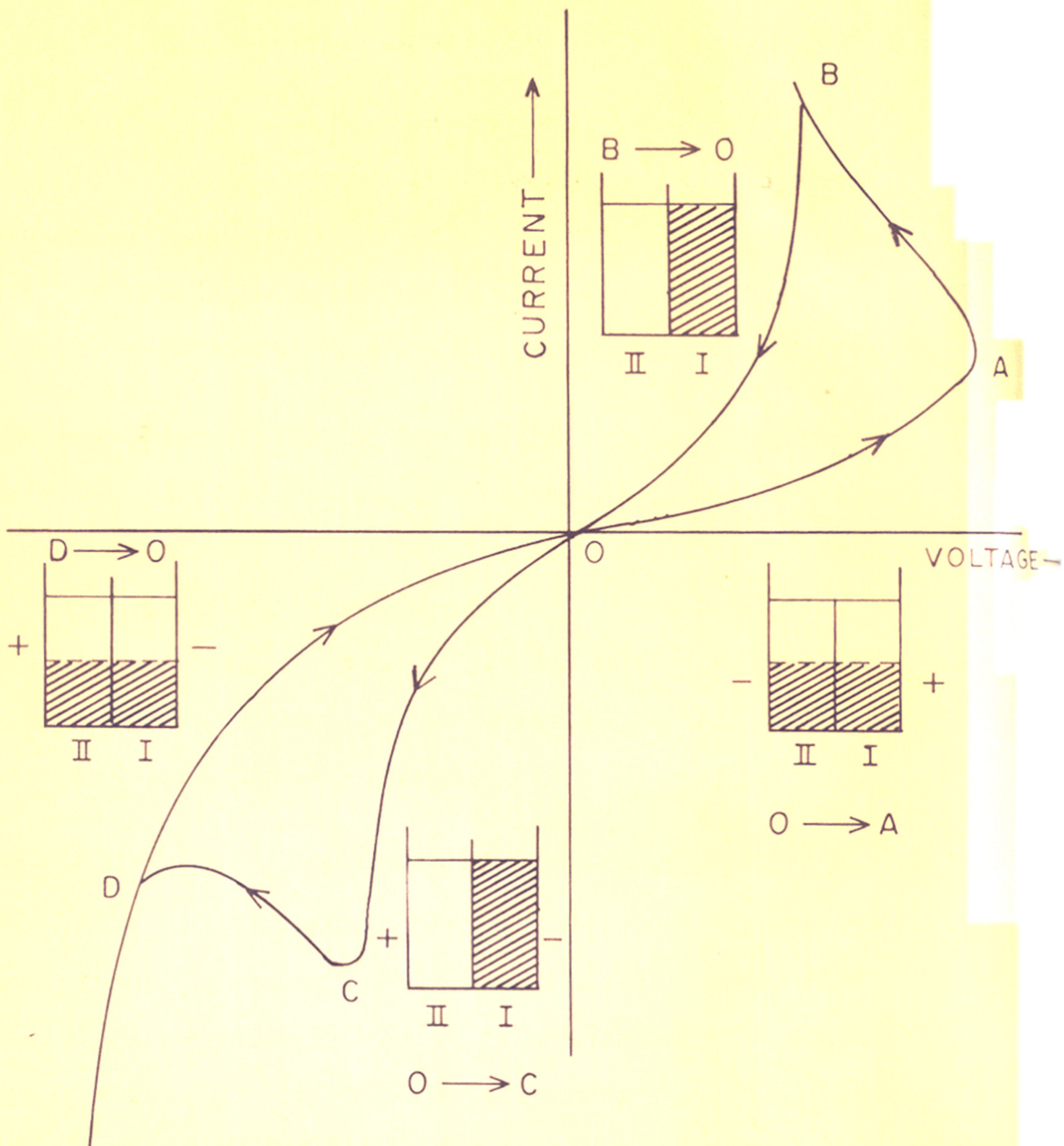
We postulate that the levels for [LEC] centres are present near the bottom electrode while those of [HEC] centres are more or less, distributed over the remaining bulk of the cadmium sulphide film. The presence of excess [LEC] centres in the vicinity of the bottom electrode is likely to be due to the vacuum deposition procedure used in the preparation of a sandwich structures. These centres as described earlier, are likely to be due to excess of Cd vacancies in the first few layers of deposited CdS whereas in the bulk of CdS we get [HEC] centres presumably due to excess of S vacancies.

Let us assume that to start with (after the irreversible breakdown) we are in the low conductivity state and the electrons are distributed equally in both the [HEC] and [LEC] centres (Fig.30 b). But the [HEC] centres are effective for electron trapping as their electron capture cross section is large. Furthermore, aluminium and indium give Ohmic contacts to such n-type vacuum deposited films. Under this situation the space charge-limited current is possible. But here [HEC] centres

being partially empty, are effective as traps and hence only a fraction 'θ' (<1) of the injected carriers will be available for conduction. This will give a situation similar to a case for the SCL law in presence of traps, as mentioned earlier. This trap distribution will remain unaltered as direct transitions between the two centres are not possible at low fields. Therefore, the same conductivity state is maintained. This state in which the [HEC] centres are partially filled is the "Low conductivity state" (Fig. 30 b).

At higher voltage when the bottom electrode is made negative, the electrons bound to [LEC] centres tunnel to [HEC] centres. This transition probability is governed by the electron capture cross section of the respective centres. For [HEC] centres it is more than for [LEC] centres and hence the tunneling is facilitated when a negative voltage is applied to bottom electrode and not in the reverse direction. The tunneling of electrons from [LEC] centres to [HEC] centres takes place only when a threshold voltage (V_A) is applied. Similar tunneling mechanism for F and V centres has been reported by Dexter[37].

After this tunneling, the [HEC] centres are nearly filled with the electrons, while [LEC] centres are nearly empty (Fig. 30 c). So [HEC] centres are no longer effective in trapping the injected electrons giving rise to increase in 'θ' . Therefore, the SCL current density increases. When we decrease the voltage the tunneling back is not possible, because of the restriction due to the relative capture cross sections as described above. The redistribution between these two types of centres does not take



I - [HEC] CENTRES II - [LEC] CENTRES

OCCUPIED UNOCCUPIED

Fig. 31. SCHEMATIC I-V CHARACTERISTIC FOR D

place and thus the electrons remain in the [HEC] centres. This gives the 'High conductivity state' (Fig.30 C).

In the high conductivity state the transfer of electrons back to [LEC] centres is difficult at lower voltage, but when the negative voltage on the top electrode is increased sufficiently, the tunneling probability of electrons from [HEC] centres to [LEC] centres increases because of two reasons; namely (i) the field is high enough to take care of the difference of capture cross sections of the two centres and (ii) the electron density of [HEC] is larger than that in [LEC] centres. Once the tunneling back to [LEC] centres takes place then the number of empty [HEC] centres increases, giving rise to decrease in θ and hence the conductivity decreases as described earlier for the low conductivity state.

The process can be described briefly as follows (Fig.31): Initially the distribution of electrons in [HEC] centres and [LEC] centres is same and 'θ' is small, due to large number of empty [HEC] centres. At V_A the tunneling of electrons from [LEC] to [HEC] centres takes place and 'θ' increases as the density of empty [HEC] centres decreases. This transforms the structure into high conductivity state. We remain in the high conductivity state until voltage V_C at which tunneling back to the empty [LEC] centres takes place, giving decrease in 'θ' as the density of empty [HEC] centres increases and the structure transforms to low conductivity state. During the low to high conductivity transformation, the current does not increase suddenly but due to increase in conductivity same current can be drawn at lower

voltage and the voltage across the sample drops to V_B. This gives the CCNR region. While during the change of high to low conductivity state, to have the same amount of current through the sample, higher voltage is necessary and hence the voltage increases to V_D. This gives VCNR region.

The above model is supported on the following grounds:

(1) Existence of such [HEC] and [LEC] centres have been established by Rose[98] and Bube[97] in CdS. Rose has explained the photoconduction on the basis of a "Activation stage", in which the transformation of electrons from [LEC] to [HEC] centres takes place. This increases the life time of the electrons and hence the photosensitivity. This activated state is similar to our "High conductivity state". The difference is that the activation in our model is achieved by tunneling of electrons while in the other case it is due to photo-excitation of carriers. Holes so generated, trap the electrons from [LEC] centres, while the density of electrons in [HEC] centres increases, due to increased number of electrons in the conduction band. In our case 'θ' increases giving rise to high conductivity, while in Rose's model the life time of electrons increases giving higher sensitivity. In our model the low conductivity state is achieved by tunneling back the electrons from [HEC] centres to [LEC] centres; while in Rose's model this is achieved by infrared quenching. The superlinearity observed in CdS photoconductors also supports these two types of centres.

(2) The two centres are characterised by the change in 'θ' only, so that the conduction is governed by the space-charge-limited law in both the conductivity states. This explains the observed current voltage characteristic in the post-breakdown stage. The nature of the log-log plot in the both states shows an Ohmic region (low voltage) due to free carriers in thermal equilibrium with traps, at high voltage when the injected electron density is large SCL law is obeyed.

(3) It is possible that the [LEC] centres are localized over a narrow region and the tunneling takes place when a critical voltage is applied across this region only. This explains the requirement of the critical voltage rather than a critical field across the sample for the transformations.

(4) Al and In play quite a significant role in this dual negative resistance phenomenon. First of all, they make it possible to inject sufficient number of electrons in the conduction band to have space-charge-limited currents. Secondly, the 'forming' gives changes in the sample and the reason may be that the destruction of the defects (which are already described earlier) present in the bulk. This destruction requires high density of carriers which is possible with aluminium and indum.

(5) Most of the other observed features can also be explained on the basis of the above mentioned model.

The existence of DNR at low temperatures can be explained because the tunneling is possible even at these temperatures. However, the current-decreases as the temperature decreases, because of the decrease in the thermally generated carrier density.

If we visualise the electron transfer as a charge transfer, this will give rise to some rearrangement of ions. This ionic adjustment will be slow. This explains the dependence of the nature of I-V curve on the frequency of the applied voltage. If the duration of the voltage is small, higher voltages are necessary to achieve complete transformation and thus increase in frequency will increase the V_A and V_D but no appreciable change is observed in V_B and V_C.

S U M M A R Y

S U M M A R Y

Aluminium-cadmium sulphide-aluminium thin film sandwiches were prepared by vacuum deposition techniques. Metal, cadmium sulphide and metal films were deposited sequentially on a thoroughly cleaned microscopic glass slide by using proper masks so as to form a crossed structure. The metals were deposited in a vacuum of the order of 10^{-6} mm. of Hg. from a tungsten filament. The following method was used for cadmium sulphide deposition. Small cadmium sulphide pellets or single crystals grown by vapour deposition technique were kept in tungsten filament. After baking at 200°C for 1/2 hour in the vacuum of the order of 10^{-6} mm.Hg, the cadmium sulphide was deposited in the vacuum at the order of 10^{-3} - 10^{-4} mm. of Hg. on the substrate at room temperature.

The current-voltage (I-V) characteristic was studied by using a simple circuit. A low frequency function generator and a 12 volt-battery with a variable potentiometer were used as sources. Tektronix Type A 515 Oscilloscope was used as a recorder. For measurements at various temperatures a brass sample holder with proper electrical contacts was used.

The structures (Al-CdS-Al) showed two stages. In the first (or pre-break down) stage the characteristic showed high resistance and hysteresis when the bottom electrode was made negative and the current varied non-linearly with voltage at higher voltages. After increasing the applied voltage beyond a critical point, which depends upon the thickness, the temperature and the nature of the

cadmium sulphide film; an irreversible break down took place and the structure was transformed into a second (or post-break down) stage. In this stage a new phenomenon of dual negative resistance was observed. Both the types i.e. current controlled negative resistance (CCNR) as well as voltage controlled negative resistance (VCNR) were observed in the same sample (Fig.17). The phenomenon can be described as follows: If the voltage was increased with top electrode positive then at V_A, the voltage across the sample suddenly dropped down to V_B through AB. On decreasing the voltage from point B the path BOC was followed. At C (top electrode negative) the current dropped down to I_D and the path DEDOA was obtained. The part of the curve OABO resembled the current controlled negative resistance curve with large hysteresis effects and the part of the curve OCDEO resembled the voltage controlled negative resistance with large hysteresis effects. At V_A, the structure transformed from low to high conductivity state while at V_C, the high to low conductivity state transformation took place. In both the states the current varied non-linearly with voltage in either direction. Furthermore, the switch over from one to the other state took place at the respective critical voltages only. If these critical voltages were not reached the I-V curve were retraced reversibly in the original state.

In order to understand the possible mechanism of this behaviour and the possible cause for the assymetry in the structure some more experiments were carried out, and the following results were obtained.

The presence of either Al or In was found to be necessary for the dual negative resistance.

The effect of temperature on this behaviour was found to be more pronounced in the pre-breakdown stage. The decrease in temperature in general increased the break down voltages V_X and the critical voltages V_A and V_D. The current density increased as the temperature was decreased.

The effect of thickness on the pre-break down stage was found to be more pronounced than the post-break down stage. The V_X increased with the increase in thickness.

It was thought that the thin aluminium oxide layer on bottom electrode and cadmium oxide film on CdS was responsible for the assymetry. To confirm this $Al-Al_2O_3$ - CdS-Al structures were prepared by growing a thin oxide film on bottom aluminium by oxidation prior to cadmium sulphide deposition and the I-V characteristics were studied. Similar structures by growing a thin oxide layer on cadmium sulphide prior to deposition of top aluminium were also prepared and studied. Furthermore, samples were prepared without breaking the vacuum between each successive deposition. All these experiments did not change the characteristics. This shows that the phenomenon as well as the assymetry may not be due to the surface layers.

The vacuum deposited films were heated in vacuum and sulphur atmosphere to remove possible non-stoichiometry. No effect was observed on DNR; however, small changes in the conductivity were observed in the pre-breakdown stage.

The original cadmium sulphide powder was mixed with In_2S_3 and Ag_2S and the samples were prepared. The adding up of impurities did not show any pronounced effect on the characteristic. The only effect was that sometimes for the samples doped with Ag_2S CCNR was observed where VCNR would have been in pure CdS and vice versa.

The study of the current-voltage dependence in the pre-breakdown stage shows that conduction can be explained on the basis of one carrier space-charge limited currents in presence of (i) free carriers in thermal equilibrium with traps, and donors, and (ii) shallow traps, the density of which increases as the distance from the conduction band increases.

The observed effects of different parameters on the pre-breakdown and post-breakdown stages show that the pre-breakdown stage is governed by the bulk of cadmium sulphide while in the latter stage the bulk has very small effect on the conduction. The cause for the transformation is suggested to be due to thermal or field breakdown which removes the effective trap density giving increased conductivity.

The conduction in the post-breakdown stage is explained on the basis of one carrier space-charge limited currents in presence of free carriers in the conduction band.

The observed DNR can be explained by one of the following two mechanisms:

(1) Formation of high field domains at critical voltage V_C transforms the structure to low conductivity state and they are destroyed at V_A transforming the structure to high conductivity state. The formation of high current filaments at V_A and disappearance of them at V_C also can explain the behaviour.

(2) Cadmium sulphide contains two types of centres:

(i) with high electron capture cross-section [HEC] and (ii) with low electron capture cross-section [LEC] . [HEC] centres are effective in trapping and are distributed in the bulk of the film while [LEC] are ineffective as electron traps and concentrated near the bottom electrode. To start with, both the [LEC] and [HEC] centres are equally populated giving a number of unoccupied [HEC] centres. This is the low conductivity state. When the negative voltage on the bottom electrode is increased (at V_A) the tunneling of electrons from [LEC] centres to [HEC] centres takes place. This decreases the density of unoccupied [HEC] centres giving decreased trapping and thus the conductivity increases. This is the high conductivity state. This state remains till the voltage in the other direction (V_C) is reached where tunneling back from [HEC] centres to [LEC] centres takes place to give a situation as in the low conductivity state. In the low conductivity state the unoccupied [HEC] centres are more than that in the high conductivity state and hence the trapping of injected and free carriers is more.

R E F E R E N C E S

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