SOME ELECTRICAL AND PHOTOCONDUCTING STUDIES ON THIN FILM CdSe AND CdTe SANDWICH STRUCTURES

A THESIS SUBMITTED

TO

THE UNIVERSITY OF POONA

FOR

THE DEGREE OF DOCTOR OF PHILOSOPHY

(IN CHEMISTRY)

BY

BOZIDAR M. ANTIC

NATIONAL CHEMICAL LABORATORY, POONA.

MAY, 1969.

ACKNOWLEDGEMENTS

I wish to express my sincere gratitude to Dr. A.P.B. Sinha for his deep interest, valuable guidance and constant encouragement throughout the course of this investigation.

My thanks are also due to Dr. C.A. Menzies for his kind help in instrumentation.

I am grateful to the Ministries of Education, Governments of India and Yugoslavia, also to the Council of Research Institute of Chemistry and Technology, Belgrade, Yugoslavia, for award of Research Fellowship.

Finally my thanks are also due to the Director, National Chemical Laboratory, Poona, India, for providing all the necessary facilities.

B. Antic

(Bozidar M. Antic)

. . .

C O N T E N T S

Page No.

...

PREFACE

With the advent of microminiaturisation in electronics, a lot of interest has been created in devices based on thin films of semiconductors. The physics of thin films offers a challenging field of research because in such films the intricate properties of surfaces play a dominant role. The behaviour of semiconductors is no longer governed so much by the familiar bulk properties of the solid, but rather by their surface properties. Such properties, though fairly well-studied for common semiconductors such as silicon and germanium, are not so well-studied for the compound semiconductors, which during recent years have been attracting considerable interest in view of their wide range of properties. Amongst such materials are cadmium selenide and cadmium telluride which, beside cadmium sulfide, are most interesting II-VI compounds, known for their versatile properties such as photo-conductivity, electroluminescence, electro-acoustic effect, field-effect and others.

The study of high field effects in thin films of these materials as well as other solids have attracted

a great number of investigators. An interesting new observation is the existence of the differential negative resistance in some semiconductor film sandwiches. As this effect is not fully understood, we started investigation in this field and have found interesting switching and memory effects in certain metal-CdSe/CdTe-metal sandwiches. In addition, these sandwiches have been found to show interesting photoeffects.

In what follows the results of experimental investigations of these sandwiches are reported and a possible explanation of the observed behaviour is presented.

In Chapter I, first the general principles of the semiconductor surface physics are given followed by a literature survey of the work done on differential negative resistance, switching and memory effects in thin films. This is followed by a brief account of the fundamental principles of photoconductivity in semiconductors. Finally, at the end of this chapter, some general properties of CdSe and CdTe including literature survey of the work done on their thin films have been brought out.

Chapter II deals with the experimental techniques which have been used in this study.

In Chapter III the experimental results are presented. Side by side, these results are discussed in relation to the work done by others to bring out a suitable explanation of the observed behaviour.

. . .

CHAPTER - 1

INTRODUCTION

It is well-known that theoretical concepts developed for infinite crystals are useful only when one is studying the bulk properties of large crystals. However, in experimental situations such as ours, where semiconductor is thin and contact effects important, one is more concerned with the conditions in the immediate vicinity of the semiconductor surface. In what follows we, therefore, discuss briefly the theory of semiconductor surface and contacts for further use in the analysis of our own experimental data.

1.1. SEMICONDUCTOR SURFACE

Tamm[1] (1932) was the first to analyse the effect of the finite size of crystal on its band structure. He found that this leads to the creation of allowed levels in the forbidden band and these states are localised at the surface. These surface states have since been studied in detail by Shockley[2] (1939), Bardeen[3] (1947) and various other workers.

The existence of surface states with energy levels in the forbidden gap gives rise to a distortion

of the band near the surface and this creates a potential barrier. Figure 1.1 shows such a barrier for an n-type semiconductor. When equilibrium is established some electrons from the bulk semiconductor fill the empty "surface states" because they lie lower in energy. This gives the surface a net negative, charge and the bulk semiconductor an equal positive charge. Whereas the negative charge is localised on the surface, the positive charge extends over a finite depth in the semiconductor. This charge disturbance leads to a band bending as shown in the figure and a barrier of height, eV_D (as seen from the semiconductor) is created. V_D is known as diffusion potential and λ_o is the width of the barrier region. The other symbols have the following meaning :

χ = Electron affinity of the semiconductor.

E_C = Energy corresponding to the bottom of the conduction band.

E_F = Fermi level.

E_V = Energy corresponding to the top of the valence band.

ϕ_{ns} = $E_C - E_F$ at the surface.

ϕ_{ps} = $E_F - E_V$ at the surface.

ϕ_s = Thermionic work function of the semiconductor.

ϕ_n = $E_C - E_F$ in bulk.

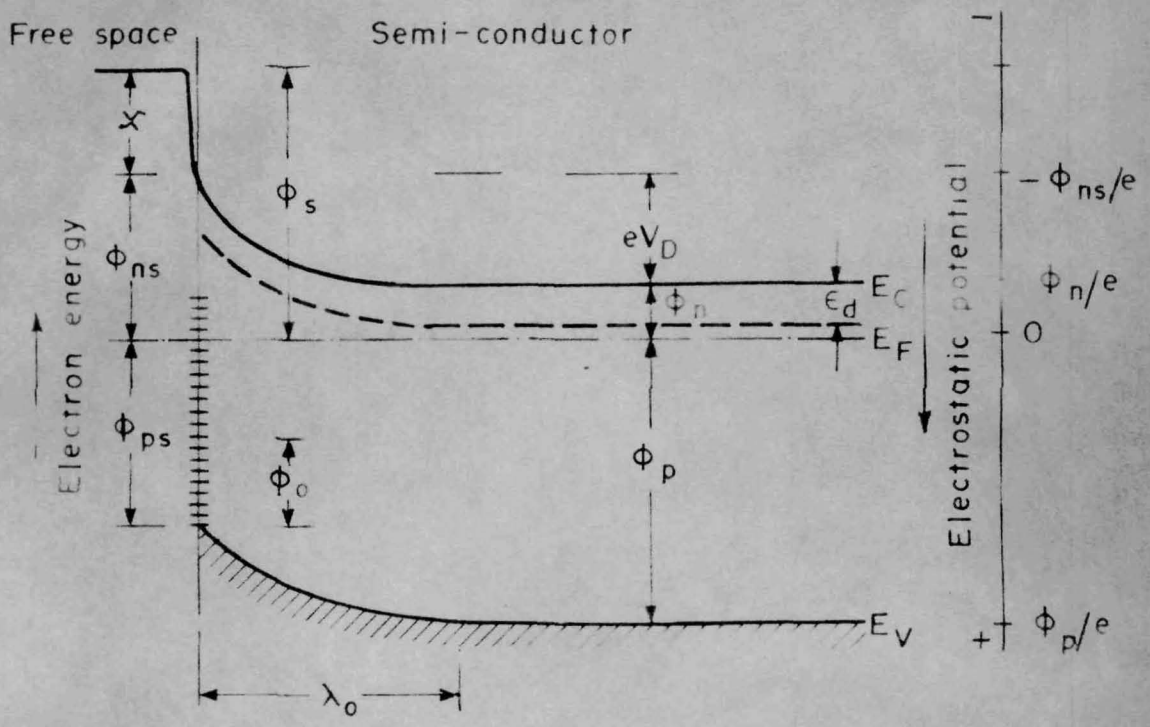


FIG. 1.1. FREE SURFACE OF AN n-TYPE SEMICONDUCTOR
(Hanisch)[4]

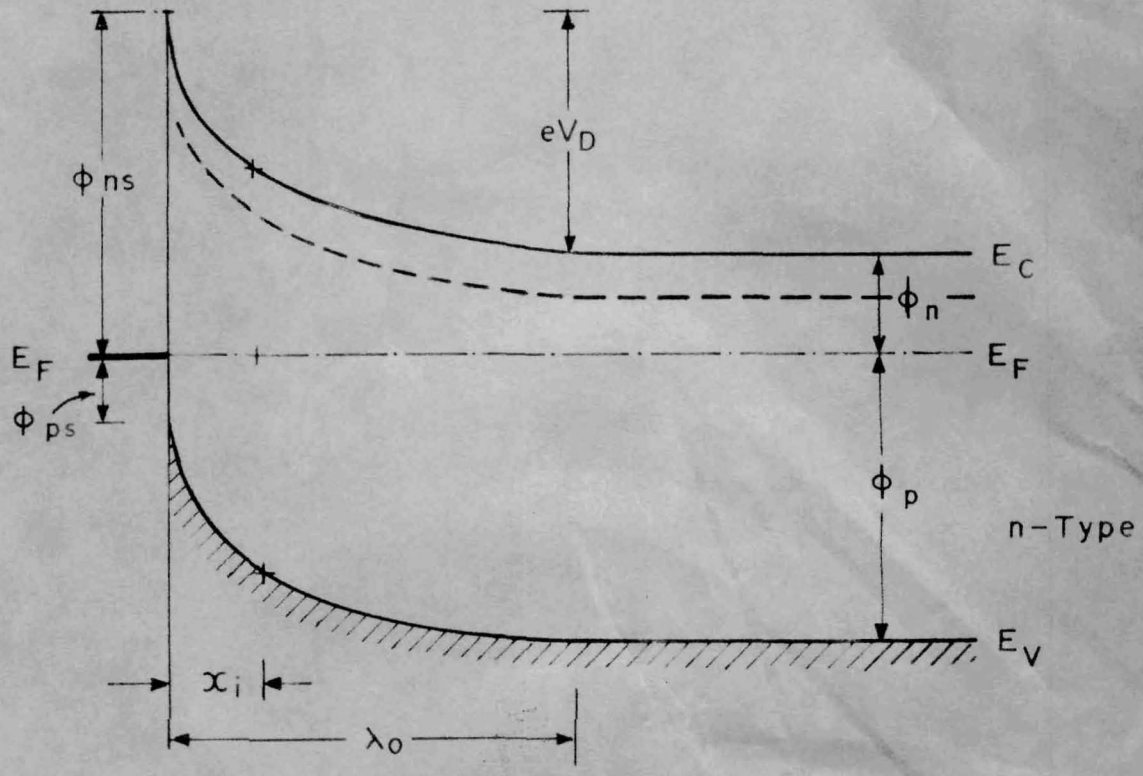


FIG. 1.2. CONTACT BARRIER WITH INVERSION LAYER (n-type
(Hanisch)[4]

ϕ_p = $E_F - E_V$ in bulk.

ϵ_d = Activation energy for the donors.

In the region near the surface all donors can be regarded as ionised. This is called the "exhaustion region". In the space charge region immediately following this, only a part of the donors are ionised and this region is called the "reverse region". Here the space charge density is a function of x, the distance from the surface.

The height (eV_D) and the thickness of the barrier (λ_o), can be calculated from the following two equations deduced under certain simplifying assumptions :

$$V_D = 2\pi N_d e \lambda_o^2 / K$$

and

$$V_D = (\phi_p - \phi_o)/e - N_d \lambda_o / 2eD_s$$

where ϕ_o = Energy interval over which the surface states of an n-type semiconductor are filled in the neutral condition.

N_d = Donor density.

K = Dielectric constant.

D_s = Density of surface states within the forbidden band (assumed constant, independent of energy).

In the above example, we have treated a case where the Fermi level is nearer to E_C than to E_V everywhere in the semiconductor. This condition is violated if the barrier height approaches the width of the forbidden band (Figure 1.2). In this case, at a point $x = x_i$ the Fermi level is in the middle of the forbidden band and for $x > x_i$ it is closer to E_C whereas for $x < x_i$ it is closer to E_V. The region between the surface and x_i is called the "inversion region" because in this region the carrier of the opposite type predominate (holes in this particular case). The inversion layer has therefore the opposite character (p-type) and effectively a p-n junction gets established.

If the band, instead of bending upwards (as shown above), bends downwards, then an enrichment or accumulation layer is formed. In this case the majority carrier concentration is higher at the surface than in the bulk.

Whatever has been said above for n-type semiconductors applies equally well to p-type semiconductors with appropriate changes in the symbols. In this case the inversion layer is formed with the

band bent downwards at the surface and the accumulation layer with the band bent upwards.

The surface states are sometimes classified as "slow states" or "fast states" depending on their relaxation time. When the density of charge in the surface states is disturbed, then, in the case of fast states, the original density is re-established immediately after the removal of the disturbance, whereas for the slow states it takes a long time. The states which are in good electrical contact with the bulk are "fast" whereas the "slow" states are thought to lie in some insulator-like layer, formed on the semiconductor surface (e.g. oxide skin). The large time constant of slow states is due to the long time taken for the charge to pass through the insulators.

1.2 METAL SEMICONDUCTOR CONTACT

(a) In absence of charged surface states

Figure 1.3(a) shows the energy level diagram of a metal and an n-type semiconductor before they have been brought in contact. Here ϕ_m is the thermionic work function of the metal. The Fermi level in the metal is taken to lie lower than that in the semiconductor (i.e. $\phi_m > \phi_n + \chi$). When they are brought in contact and the electronic equilibrium established, the Fermi levels in the two materials must coincide, on thermodynamic grounds. To achieve this, electrons must flow from the semiconductor to the metal, raising the Fermi level in the metal with respect to that in the semiconductor. The energy diagram now is as shown in Figure 1.3(b). Due to the charge flow, a potential difference equal to $\phi_m - (\phi_n + \chi)$ has been created at the contact, which is known as the contact potential. Whereas the negative charge is localised on the surface, the corresponding positive charge (i.e. ionised donors) is distributed over a region in the semiconductor adjacent to the contact. The height of the barrier as seen from the metal side is $\phi_{ns} = \phi_m - \chi$ and as seen from the semiconductor is

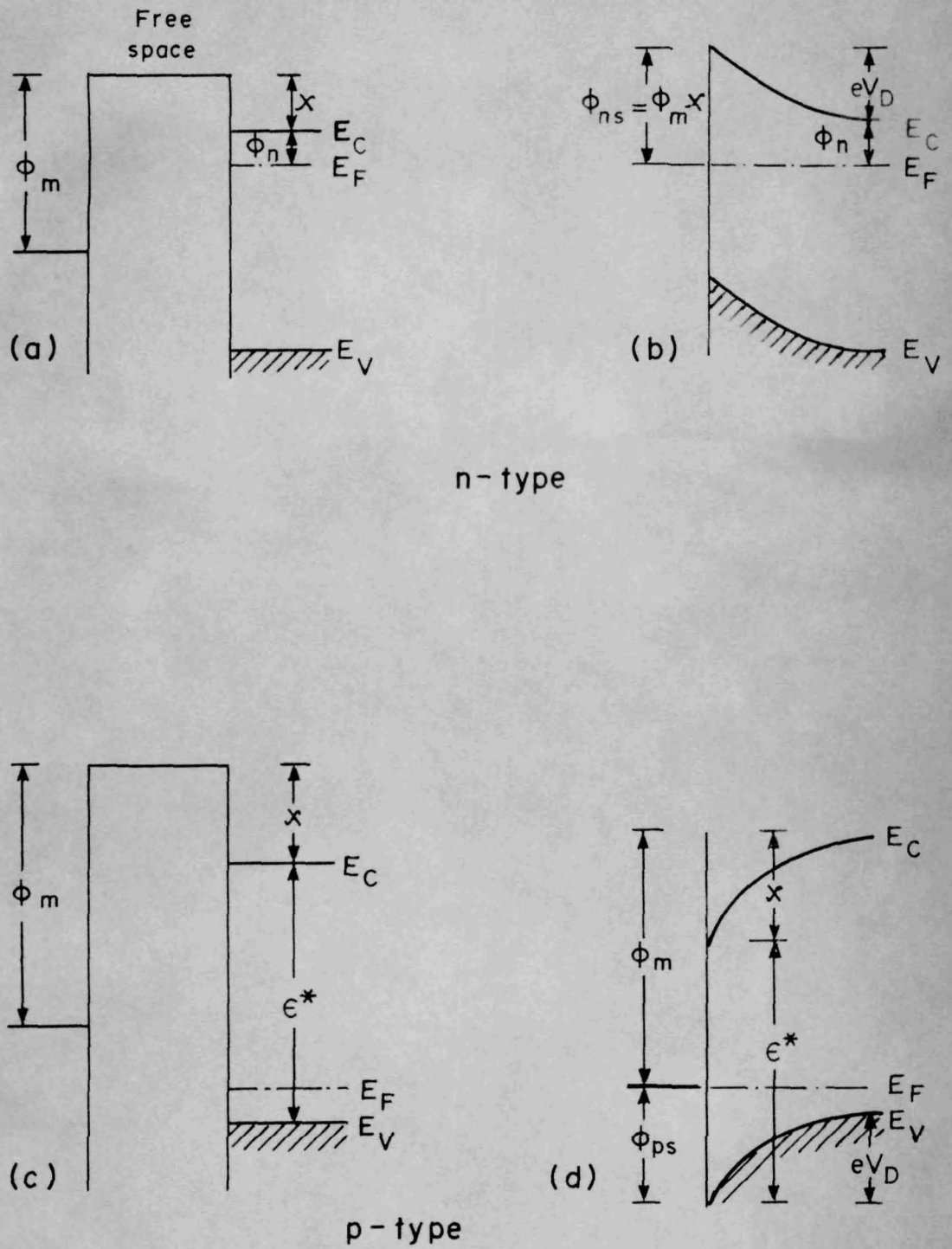


FIG. 1.3. METAL-SEMICONDUCTOR CONTACT IN THE ABSENCE OF SURFACE STATES

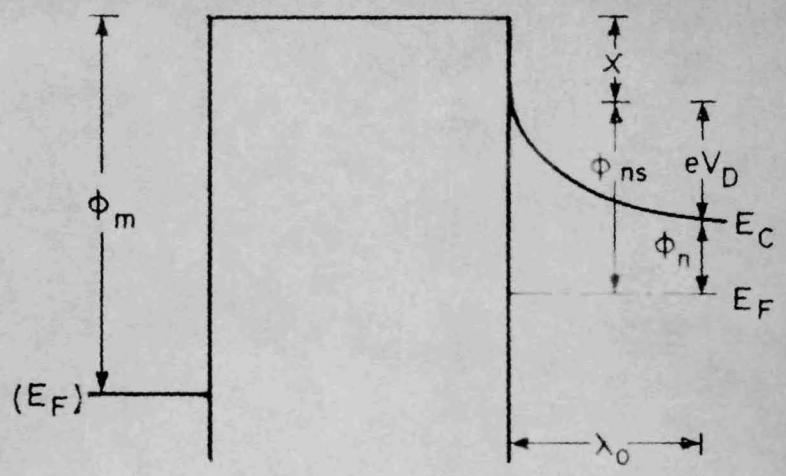
(Henisch)[4]

$eV_D = \phi_m - (\phi_n + \chi)$. Figure 1.3(c) and (d) show the corresponding curves for the p-type materials.

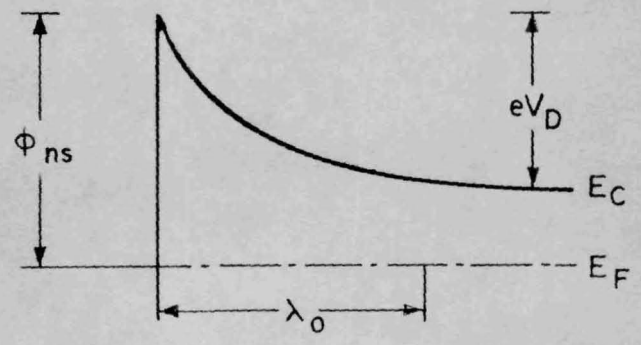
(b) <u>In presence of charged surface states</u>

The energy profile in presence of charged surface states is different from what has just been described due to the fact that there already exists a barrier before the contact is established. As before, when contact is established, electrons must flow (in the case with $\phi_m > \phi_n + \chi$) to the surface of the metal in order to raise its Fermi level. However, the essential difference arises from the existence of a large reservoir of electron at the surface of the semiconductor in the surface states. This reservoir is able to provide the electrons without disturbing significantly the already existing space charge in the semiconductor. λ_o and eV_D are therefore almost independent of ϕ_m and ϕ_s (Fig. 1.4 a, before contact and b after contact).

Intermediate cases may arise when the density of surface states is not large enough to make λ_o and eV_D entirely independent of ϕ_m and ϕ_s.



(a)



(b)

FIG. 1.4. METAL–SEMICONDUCTOR CONTACT IN THE PRESENCE OF SURFACE STATES (n-type) *(Henisch)*[4]

1.2.i EFFECT OF AN EXTERNAL APPLIED VOLTAGE ON CONTACT BARRIER

When an external voltage U is applied to a metal-semiconductor-metal system, the voltage drop is distributed over the two contacts and the bulk depending upon the relative resistances of the three regions. The voltage drop across a semiconductor-metal contact (designated as V_B) displaces the Fermi level at $x = \lambda$ with respect to that at $x = 0$ by an amount eV_B (Fig. 1.5). The height of the barrier as seen from semiconductor increases by eV_B when V_B is positive and decreases when V_B is negative (for n-type semiconductors and vice versa for p-type). The thickness of the barrier λ can be found by using Poisson's equation and is given by :

$$\lambda = \left[\frac{\epsilon(V_D + V_B)K}{2\pi N_d e^2} \right]^{1/2}$$

where V_D is the diffusion voltage described earlier and V_B is the potential difference across the barrier layer, resulting from the application of a total external voltage U which can take either positive or negative value. This type of barrier with voltage dependent thickness was first suggested by Schottky[5] and is often

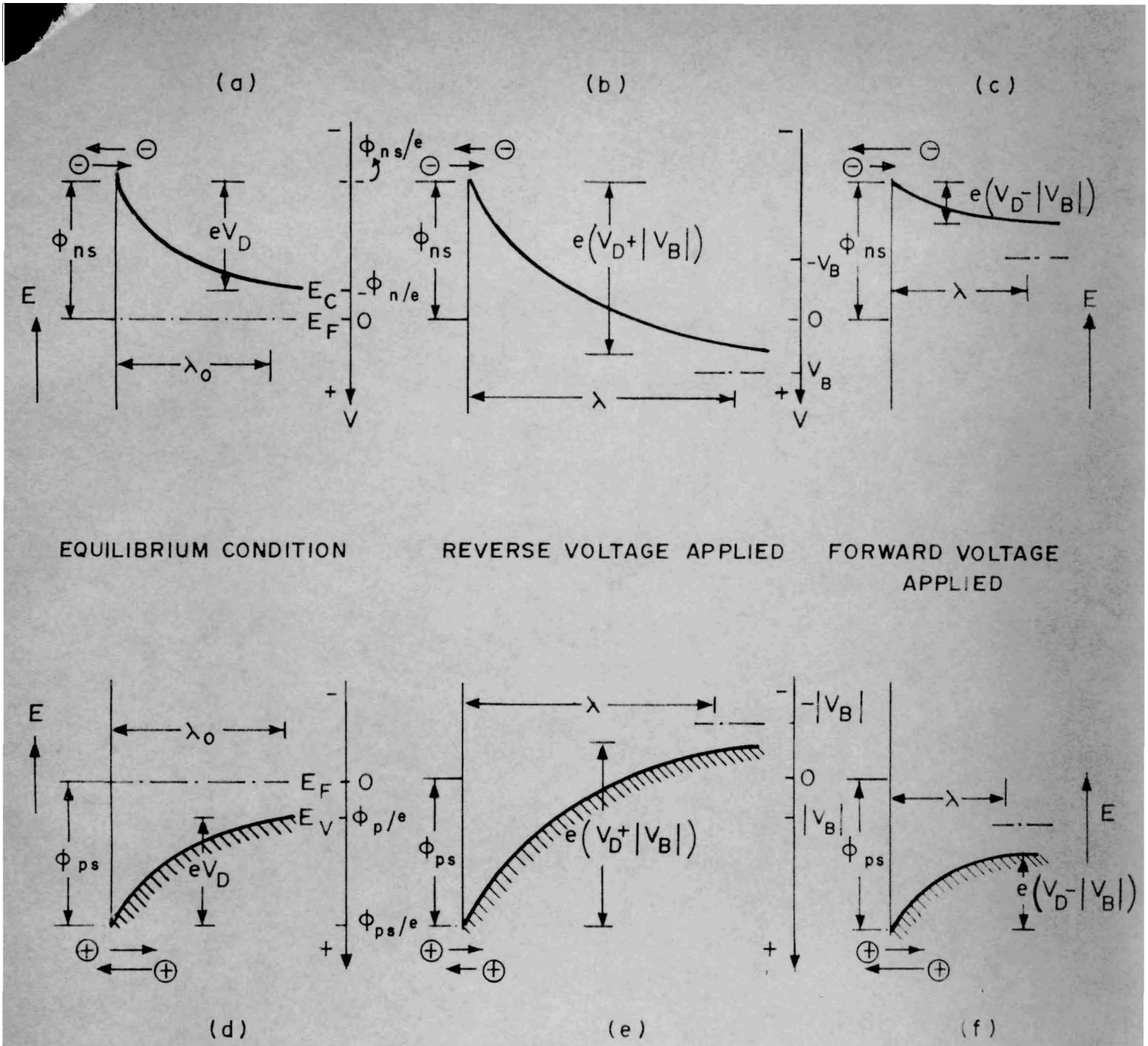


FIG. 1.5. SCHOTTKY-TYPE BARRIER UNDER THE INFLUENCE OF APPLIED VOLTAGE (a),(b),(c) n-type ; (d),(e),(f) p-type

(Henisch)[4]

called 'Schottky type barrier'. Such a barrier is formed when the donor concentration is uniform throughout the semiconductor.

The other type of barrier where its thickness is almost independent of applied voltage is called 'Mott barrier'[6] and arises when N_d is small near the surface but abruptly takes up very high value in the bulk. In this case, on application of a reverse voltage, the additional space charge is provided without extending the barrier region because the impurity content in the bulk is so high.

1.2.ii. RECTIFICATION

(a) The diode theory

If the barrier thickness is small compared to the mean free path of the carrier, then the collisions within the barrier region can be neglected. The shape of the barrier profile then becomes immaterial in the study of rectification and the current is governed entirely by the barrier height. The theory of rectification under this approximation was developed by Bethe[7] (1942) and is known as 'Diode Theory'.

In the absence of applied voltage, the number of electrons crossing from metal to semiconductor per unit time is equal to that coming in the opposite direction so a dynamic equilibrium is established. If the metal is made positive with respect to an n-type semiconductor the height of the barrier viewed from the metal remains unchanged. However, the electron levels in the semiconductor are raised by an amount $e|V_B|$. The height of the barrier viewed from the semiconductor therefore decreases by $e|V_B|$. This leads to an increased electron current from semiconductor to metal which increases exponentially with $|V_B|$. If the reverse voltage is applied again the barrier height viewed from metal side remains unchanged but that viewed from the semiconductor increases and the electron flow to the metal has decreased.

The total current flow, whatever be the direction of the applied field, is

$$J = J_s \left[1 - \exp \left(- \frac{eV_B}{kT} \right) \right]$$

where V_B has the same sign as that of the voltage applied on the semiconductor and J is positive when

positive current flows from semiconductor to metal. Here,

$$J_s = AT^2 \exp\left(-\frac{\phi_{ns}}{kT}\right)$$

where ϕ_{ns}, as already mentioned, is the barrier height as seen from the metal and A is Richardson's constant. Thus

$$J = AT^2 \exp\left(-\frac{\phi_{ns}}{kT}\right)\left[1 - \exp\left(-\frac{eV_B}{kT}\right)\right]$$

For high forward voltage (V = negative)

$$|J| \simeq AT^2 \exp\left(-\frac{\phi_{ns}}{kT}\right) \exp\frac{e|V_B|}{kT}$$

For high reverse voltage (V = positive)

$$|J| \simeq AT^2 \exp\left(-\frac{\phi_{ns}}{kT}\right)$$

which is independent of applied voltage (saturation).

These equations have been deduced under highly simplifying assumptions. For a more realistic picture, the effect of image force and tunnel penetration has to be taken into account. These corrections affect

the reverse current considerably and the modified equation becomes[4] : $J = J_s \exp \left[(V_D + |V_B|) e^7 \pi N/2K^3 \right]^{1/4} / kT$ (N = impurity density) if the effect of image force predominates and $J = J_s \exp \left[(V_D + |V_B|) 8e^3 \pi N/K \right]^{1/2} x_c / kT$ if the tunnel mechanism predominates. Here x_c is the critical thickness below which the barrier can be considered transparent to tunneling.

(b) The Diffusion Theory

Under the diffusion theory i.e. where one cannot neglect electron collisions within the barrier the shape of the barrier is important so we have two cases :

(i) Mott Barrier

In this case, J is given by

$$J = \frac{\sigma(V_D + |V_B|)}{\lambda_o} \exp \left(- \frac{eV_D}{kT} \right) \left\{ \frac{1 - \exp \left(- e|V_B| / kT \right)}{1 - \exp \left[- e(V_D + |V_B|) / kT \right]} \right\}$$

and

(ii) Schottky Barrier

In this case J is given by :

$$J = \sigma \left[\frac{(V_D + |V_B|) 8\pi Ne}{K} \right]^{1/2} \exp\left(-\frac{eV_D}{kT}\right) \left\{ \frac{1-\exp(-e|V_B|/kT)}{1-\exp\left[-2e(V_D + |V_B|)/kT\right]} \right\}$$

where σ is the bulk conductivity of the semiconductor. These equations also get suitably modified when the effect of image force and tunnel penetration is taken into account.

1.2.iii. INJECTING CONTACTS

As already mentioned, when the barrier height becomes comparable to the band gap, a surface inversion layer is formed. On an n-type bulk material, the inversion layer has the p-character and gives rise to a large source of hole supply near the surface.

Under a forward bias a large number of holes are easily injected into the bulk n-type semiconductor so that the forward current is now composed of hole current in addition to the usual electron current. The injection efficiency γ is defined as :

$$\gamma = \frac{|J_p|}{|J_p| + |J_n|}$$

and γ can lie between zero and unity. The injection ratio γ_o at low injection level has been calculated[4] and is given as :

$$\gamma_o = \frac{1}{1 + \left(\frac{e\tau_p}{2\pi\mu_p m}\right)^{1/2} \exp\left[\left(\epsilon^* - eV_D - 2\phi_n\right)/kT\right]}$$

where τ_p = Lifetime of additional holes.

μ_p = Mobility of holes.

m = Mass of electrons and holes treated as equal.

1.2.iv. OHMIC CONTACT

What has been said above is concerned with the presence of a barrier at metal-semiconductor contact. When there is no barrier at such a contact the electric conduction obeys the Ohm's law and the contact is called 'ohmic'.

Such a case arises when the metal Fermi level lies above the semiconductor Fermi level for an n-type material or in the other words when metal work function is lower than that of the semiconductor. For a p-type material, this is just the other way round i.e. the metal work function should be higher than that of the semiconductor to provide ohmic contact. However, this simple theory fails in many cases due to the complication arising from surface states, etc.

In addition, ohmic contacts are also formed when a contact is made on a degenerate semiconductor containing a large density of impurities near the surface. High impurity concentration makes the barrier extremely thin and so transparent to the carriers.

1.3 SOME OTHER FACTORS GOVERNING CONDUCTION IN THIN FILMS OF SEMICONDUCTORS OR INSULATORS

We have so far discussed the processes taking place at the semiconductor surface or at the semiconductor-metal contacts. In addition to these, the factors governing the transport of carriers across the semiconductor or insulator films are also important in determining the overall property of the metal-semiconductor-metal sandwiches. The following are some such processes which govern the conduction in thin films of insulators and semiconductors :

i) Space charge (injection carriers).
ii) Metal to metal tunneling through insulator.
iii) Tunneling through traps and impurity levels.
iv) Space charge limited tunneling.
v) Field ionisation of traps.
vi) Electrical breakdown.
vii) Schottky field emission.

Figure 1.6 shows these processes diagrametically.

1.3.1 SPACE CHARGE (INJECTION CARRIERS)

From what has been said earlier, it is clear that it is possible to inject carriers into the insulators

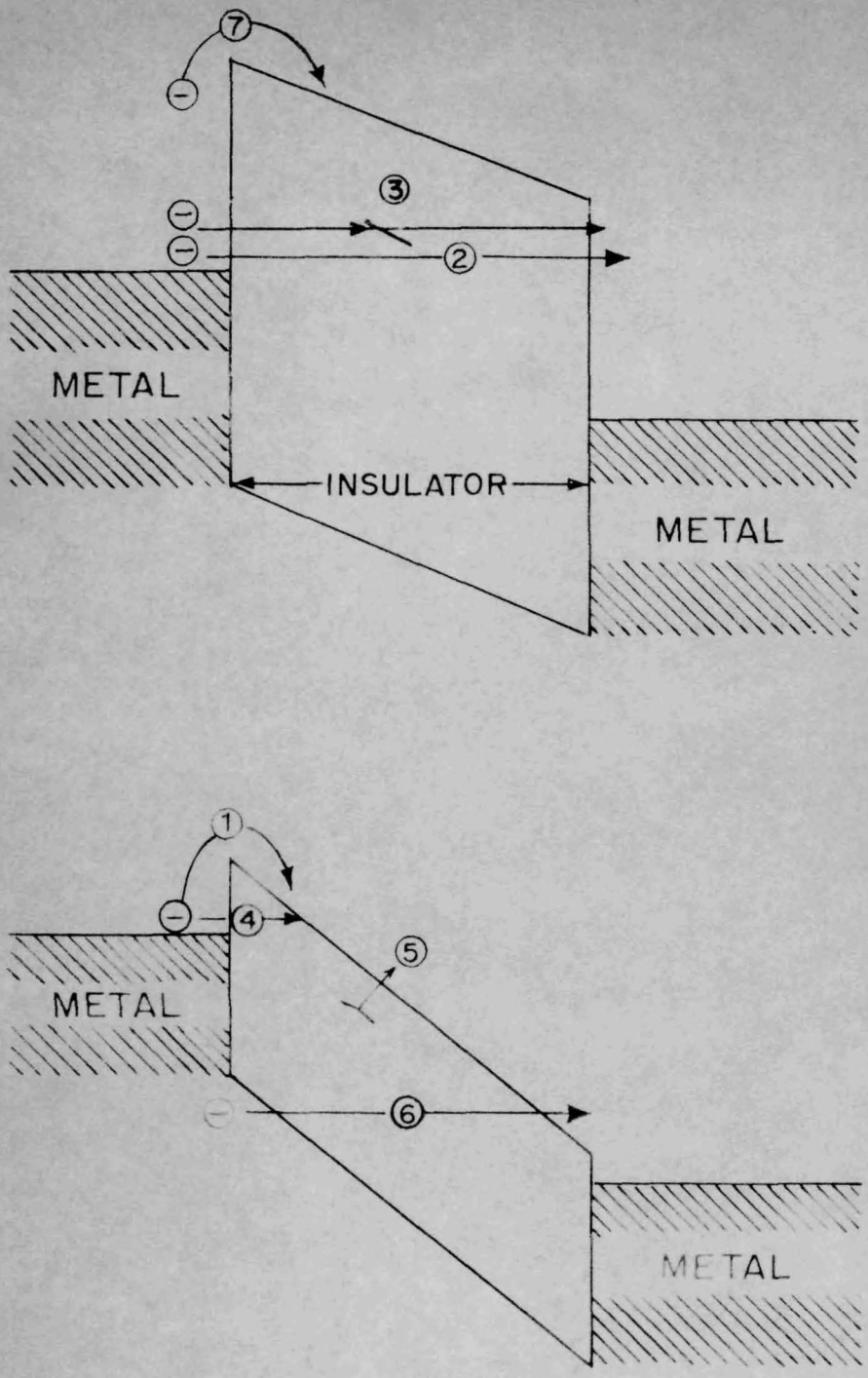


FIG 1.6. SCHEMATIC REPRESENTATION OF DIFFERENT CONDUCTION MECHANISMS IN METAL-INSULATOR-METAL DIODES.

and semiconductors from suitable contacts. The injected carriers form a space charge and further flow of current is governed by this space charge.

Mott and Gurney[8] (1940) deduced an expression for space charge limited current density J in a trap-free insulator :

$$J = 10^{-13} \mu K \frac{V^2}{d^3}$$

where : μ = Mobility of the injected carriers.

K = Dielectric constant.

V = Applied voltage.

d = Thickness of the insulator film.

Rose[9] has discussed single carrier space charge limited current in insulators with traps. This work has been followed by that of Smith and Rose[10] on space charge limited current in CdS single crystal. One carrier space charge limited current in CdS films has been reported by Zuleeg and Muller[11] and Dresner and Shallcross[12].

Extensive work on two carrier space charge limited current has been done by Lampert[13,14], Lampert and Rose[15], Parmenter and Ruppel[16].

In an excellent review, Lampert[17] gave details of two carrier space charge limited current in solids in presence of traps. He has shown that a current controlled differential negative resistance in insulator may be observed if the life time of two carriers are not equal and they are dependent on the degree of injection.

1.3.ii. METAL TO METAL ELECTRON TUNNELING

In accordance with classical principles, an electron can cross a potential barrier of height V only if its kinetic energy exceeds a definite minimum given by :

$$1/2m\upsilon^2 \geqslant eV$$

Electrons which do not satisfy this relation would be completely reflected. However, a wave-mechanical analysis of the problem shows that an electron which has insufficient energy to pass over the barrier has a definite chance of passing through it. No doubt, an electron wave function is rapidly attenuated and only very thin barriers allow electrons to be transmitted.

If two metal electrodes are separated by a thin layer of an insulator ($\sim 50\mathring{A}$), then in the absence of an applied voltage, dynamic equilibrium exists and

the rates at which electrons penetrate the barriers in opposite directions are equal. However, if one metal is made more negative than the other, then there will be a net current flow. In a simplified form, the current voltage relationship for tunneling is :

$$J = AV^2 \exp(-B/V)$$

It can be seen that the process is temperature-independent.

Tunneling has been proposed by Frenkel[18] and since then extensive calculations have been reported by Sommerfield and Bethe[19], Holm and Kirschestein[20], Holm[21], Mead[22]. Fisher and Giaver[23] have reported tunneling through Al-Al_2O_3-Al diodes. The results show that current increases exponentially with voltage and it is nearly independent of temperature.

1.3.iii. TUNNELING THROUGH TRAPS AND IMPURITY LEVELS

Conduction can also take place by the tunneling of electrons through traps and empty impurity levels in the semiconductor. A large density of such empty states located near the Fermi level offers a favourable condition for this process. Penley[24] has obtained an

expression for tunnel current through such traps for a rectangular potential barrier.

1.3.iv SPACE CHARGE LIMITED TUNNEL EMISSION

In some cases, electrons tunnel from the conduction band of the metal to the conduction band of the semiconductor after which their motion in the conduction band of the semiconductor is governed by the space charge they create.

Geppert[25] has considered the case of a rectangular potential barrier and deduced an expression for such conduction. Pittelli[26] has studied theoretically the space charge limited tunnel emission in presence of traps and observed a temperature dependence of current.

1.3.v. FIELD IONISATION OF TRAPS

Some of the filled traps can be ionised under the action of electric field and can contribute towards the density of conduction electrons. This process is known as field ionisation of traps and is significant when the trap density near the conduction band edge is large and the barrier high.

Franz[27] has shown that the current density J, due to field ionisation of traps is of the form :

$$J = A \frac{E}{E_t} \exp\left(- B \frac{E_t^{3/2}}{E}\right)$$

where : E = Electric field.

E_t = Energy of the trap level measured from the bottom of the conduction band.

A and B are constants.

Boër and Kummel[28] have studied the effect of field on conductivity of single crystals of CdS and interpreted the increase of conductivity with field as an evidence of field ionisation of trapped electron.

1.3.vi ELECTRICAL BREAKDOWN

(a) Avalanche breakdown

Von Hippel[29,30] has shown that at high electric fields, the free electrons in the conduction band are accelerated and they transfer their excess energy to electrons in the valence band raising them to conduction band and creating new electron-hole pairs. This builds up a large density of free carriers and J-V relation takes the form :

$$J = J_0 \exp(\alpha \sqrt{V})$$

For carrier collision and multiplication to take place, the film thickness must be larger than the mean free path of the carriers.

Von Hippel[31] has attributed the increase in current density of a reverse-biased p-n junction diode to this process. McKay and McAfee[32] have also reported avalanche breakdown in germanium and silicon.

(b) Zener breakdown

When a high field is applied across an insulator or a semiconductor then the band diagram bends steeply and the electron in the valence band has the same energy as an empty level in the conduction band elsewhere in the crystal. The electrons can then tunnel through the gap[33] and the current density J is of the form :

$$J = AV \exp(\alpha - \beta/E)$$

1.3.vii SCHOTTKY FIELD EMISSION

When an electric field is applied across the barrier, the barrier height is lowered due to the image force and the number of electrons crossing the barrier increases. The current density, therefore, becomes a function of applied field as well as of temperature. This is an important mechanism which we would be discussing in greater detail along with our experimental results in Chapter III.

1.4 PHOTOCONDUCTIVITY AND PHOTOVOLTAIC EFFECTS

The free electrons and holes generated by thermal ionisation have density corresponding to thermal equilibrium and are called "equilibrium carriers". Beside thermal ionisation there are other ways, such as optical excitation, which can contribute to the generation of free carriers. In contrast to thermal energy, energy used to generate the excess carriers is retained mainly by electrons and the average energy of the crystal lattice remains practically unaffected. Hence the thermal equilibrium between electron and lattice is distributed and consequently the carriers generated by light are called "non-equilibrium carriers". The total density is the sum of equilibrium (n_o, p_o) and non-equilibrium (Δm, Δp) carrier densities i.e.

$$n = n_o + \Delta n \quad \text{and} \quad p = p_o + \Delta p$$

As a result, equation for conductivity

$$\sigma = e\,(\mu_n . n + \mu_p . p)$$

becomes

$$\sigma = e\,(\mu_n . n_o + \mu_p . p_o + \mu_n . \Delta n + \mu_p . \Delta p)$$

Thus the excess conductivity due to non-equilibrium carrier density is given as :

$$\Delta\sigma = e\,(\mu_n \Delta n + \mu_p \Delta p)$$

assuming that the mobilities for equilibrium and non-equilibrium carriers are the same. It is reasonable to assume that number of electrons and holes generated in unit time and unit volume, $\Delta n'$ and $\Delta p'$ should be proportional to the optical energy absorbed in unit volume. If the intensity of light is I then quantity of optical energy absorbed in unit time in 1 cm^2 layer with thickness dx (where x is in the direction of light) is proportional to I and dx :

$$-dI = kI\,dx$$

where k is the coefficient of proportionality known as optical absorption coefficient. Then optical energy absorbed in unit time and volume is :

$$-dI/dx = kI$$

Hence $\Delta n'$ and $\Delta p'$ should be proportional to kI :

$$\Delta n' = \Delta p' = \beta k I$$

where β is the coefficient of proportionality. Furthermore, if I represents the number of quanta per sec., then β is the quantum yield i.e. the number of electron hole

pairs generated by a single quantum. If illumination starts at a certain time and if the generation of carriers is the only process taking place then the density of non-equilibrium carriers increases with time as follows (Fig. 1.7) :

$$\Delta n = \Delta p = \beta k I t$$

Dashed line in figure represents such a process.

However, it is known that after a certain time from the beginning of the illumination a steady state ($\Delta \sigma_{st}$) is established, which corresponds to the steady state of the non-equilibrium carrier densities.

The same is true when illumination is ceased; photoconductivity does not decay instantaneously but a certain time is required for that (Fig. 1.8). Rise and decay curves of the non-equilibrium conductivity (relaxation curves) may be exponential or non-exponential depending upon the nature of the recombination processes.

There are three electronic transitions which are common in photoconductors : (a) absorption and excitation, (b) trapping and capture and (c) recombination.

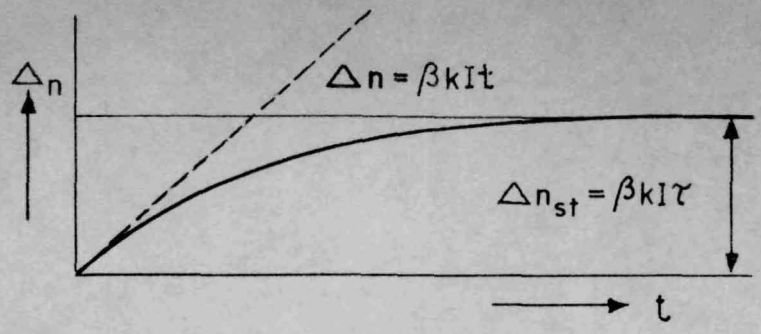


FIG. 1.7. VARIATION OF CARRIER DENSITY WITH TIME DURING ILLUMINATION.

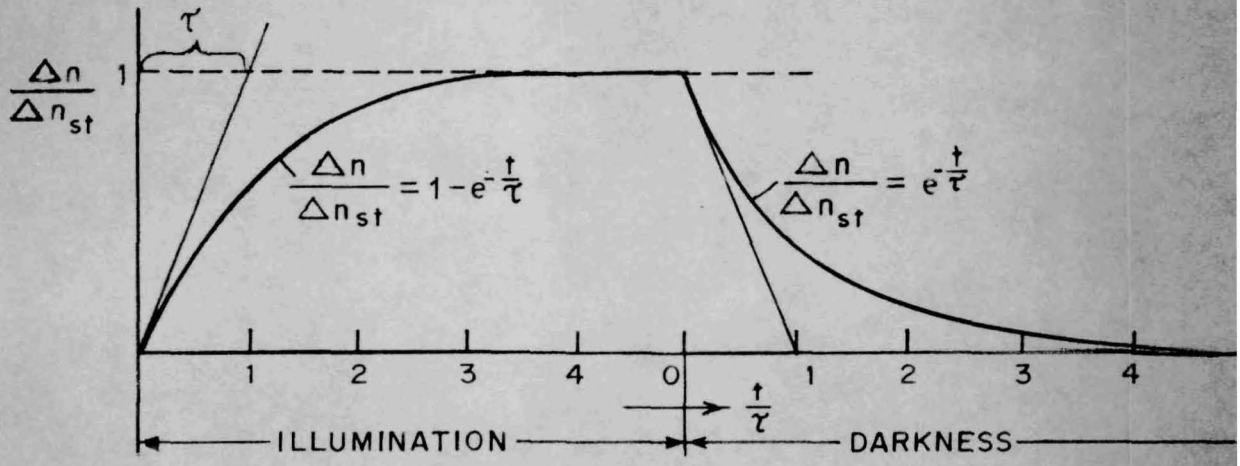


FIG. 1.8 RELAXATION OF THE NONEQUILIBRIUM DENSITY ON EXCITATION WITH A SQUARE LIGHT PULSE. LINEAR RECOMBINATION CASE *(Ryvkin)*.[34]

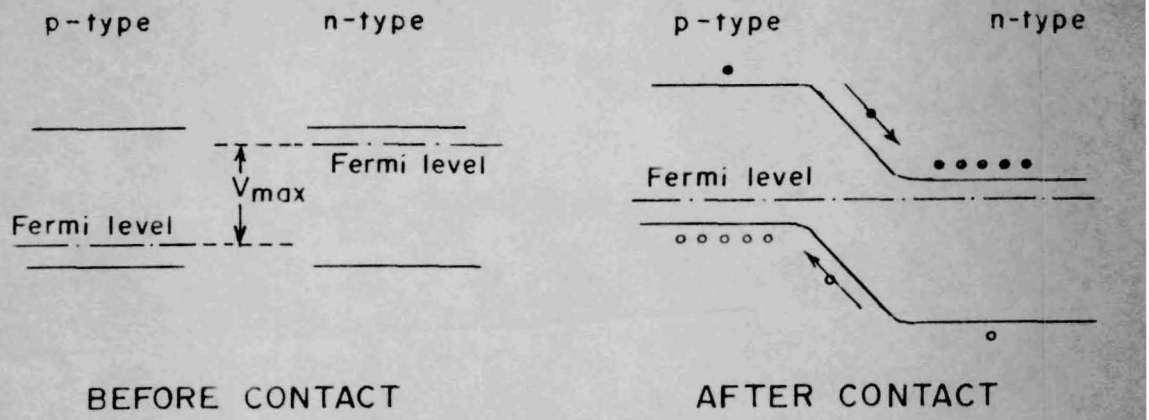


FIG. 1.9. ENERGY-BAND SCHEME FOR DESCRIPTION OF PHOTOVOLTAIC EFFECT *(Bube)*.[36]

In process (a) the excitation may take place (i) from the valence band to the conduction band producing a free electron and a free hole, (ii) from a localised level in the forbidden band to the conduction band producing a free electron or (iii) from the valence band to a localised level producing a free hole.

Once a carrier is freed it will remain free until it is captured at an imperfection or recombines directly. The direct recombination is generally less probable. The captured carriers can be either released back thermally or recombine. In the former case the centers are called "trapping centers" and in the later "recombination centers". The recombination through the recombination centers takes place when an electron is captured by an excited center containing a hole or when a hole is captured by an excited center containing an electron. These transitions may be associated with release of photons in which case they are said to be "radiative".

In steady state, the reverse rate of annihilation or recombination of carrier becomes equal to the above

rate of creation. The value of non-equilibrium carrier density, therefore, reaches a "saturation" after a certain time.

Real scientific approach to photoconductivity phenomena started with the introduction of the concept of lifetime of free carrier and the carrier capture cross-section to a bound state which according to Rose[35] were not used before 1945.

Lifetime is the time for which each generated carrier exists in free state before it combines. Free state lifetime may be very different for different carriers and often the average lifetime is used. The steady-state electron and hole density are therefore

$$\Delta n_{st} = \beta k I \tau_n \quad \text{and} \quad \Delta p_{st} = \beta k I \tau_p$$

where τ_n and τ_p are the average lifetimes of electrons and holes respectively. $\Delta\sigma_{st}$ is then given by :

$$\Delta\sigma_{st} = \Delta\sigma_n + \Delta\sigma_p = e\beta k I (\mu_n \cdot \tau_n + \mu_p \cdot \tau_p)$$

When either electron or hole predominates in a system :

$$\Delta\sigma_{st} = e\beta k I \mu \tau$$

Factors k and β represent the interaction of light with material and the process of generation of non-equilibrium carriers are governed by them. μ and τ are controlled by the interaction of the carriers with the material and represent the process of the motion and recombination of the non-equilibrium carriers.

If by some means the non-equilibrium holes and electrons (generated by light) are separated, a potential difference will arise between two portions of the material. This rise in potential is called "photovoltaic effect" and is caused due to absorption of photons in the vicinity of a potential barrier. Such a barrier may arise at a p-n junction, at the contact between metal and semiconductor, or at the junction of two semiconductors with unequal band gaps. It may also arise due to the difference between the surface and volume conductivity of a material. The establishment of the photovoltage can be described in terms of the energy level scheme for a p-n junction as shown in Fig. 1.9. The electrons generated under illumination in the p-type portion move across the barrier and similarly the holes generated in n-type portion cross the barrier and go to the p-region.

If the junction is open circuited a voltage is built up across the junction. The built-up photovoltage is of the same sign as that required to give a forward bias to the junction. It is hardly necessary to state that a p-n junction photovoltaic element is at the same time photoconducting too. Such an element biased in the reverse direction will change its reverse current characteristic under illumination i.e. the reverse current will rise. This had led to construction of photodiodes.

1.5 DIFFERENTIAL NEGATIVE RESISTANCE, SWITCHING AND MEMORY PHENOMENA

The differential electrical resistance dV/dI normally has a positive value. However, under certain conditions some materials may exibit a negative dV/dI. Tunnel or Esaki diode is based on negative resistance phenomenon and is widely used for amplifier and oscillator operations in the range of high frequencies.

There are two types of differential negative resistances; (i) a current controlled negative resistance (CCNR) Fig. 1.10, and (ii) a voltage controlled negative resistance (VCNR). In the former, which is also known as 'S-shaped', the current is multivalued at a certain voltage, whereas in the latter, which is also called 'N-shaped' the voltage is multivalued for a certain current value. Apart from negative resistance, some samples may show switching and memory effects. Figure 1.11a shows bistable conductivity state and switching. Figure 1.11b shows the same but with a memory effect. The difference between these and simple negative resistance given above is obvious from a comparison of the figures. For example, if the I-V curve is similar

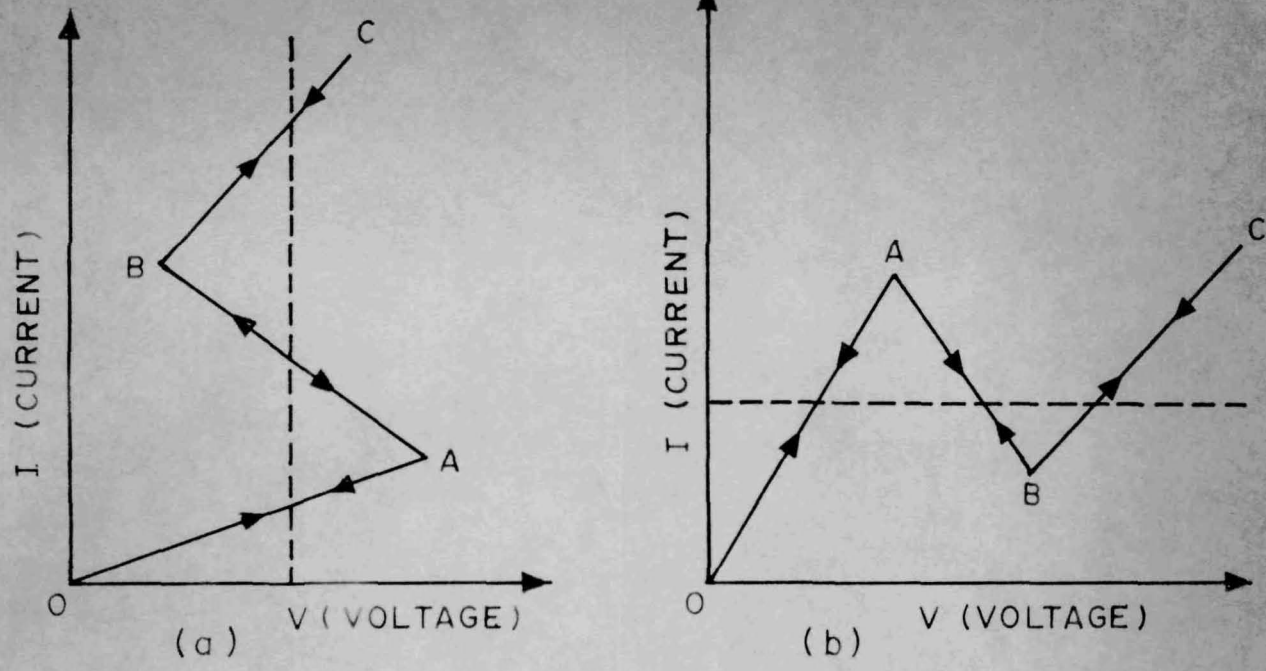


FIG. 1.10 DIFFERENTIAL NEGATIVE RESISTANCE
(a) CCNR ; (b) VCNR.

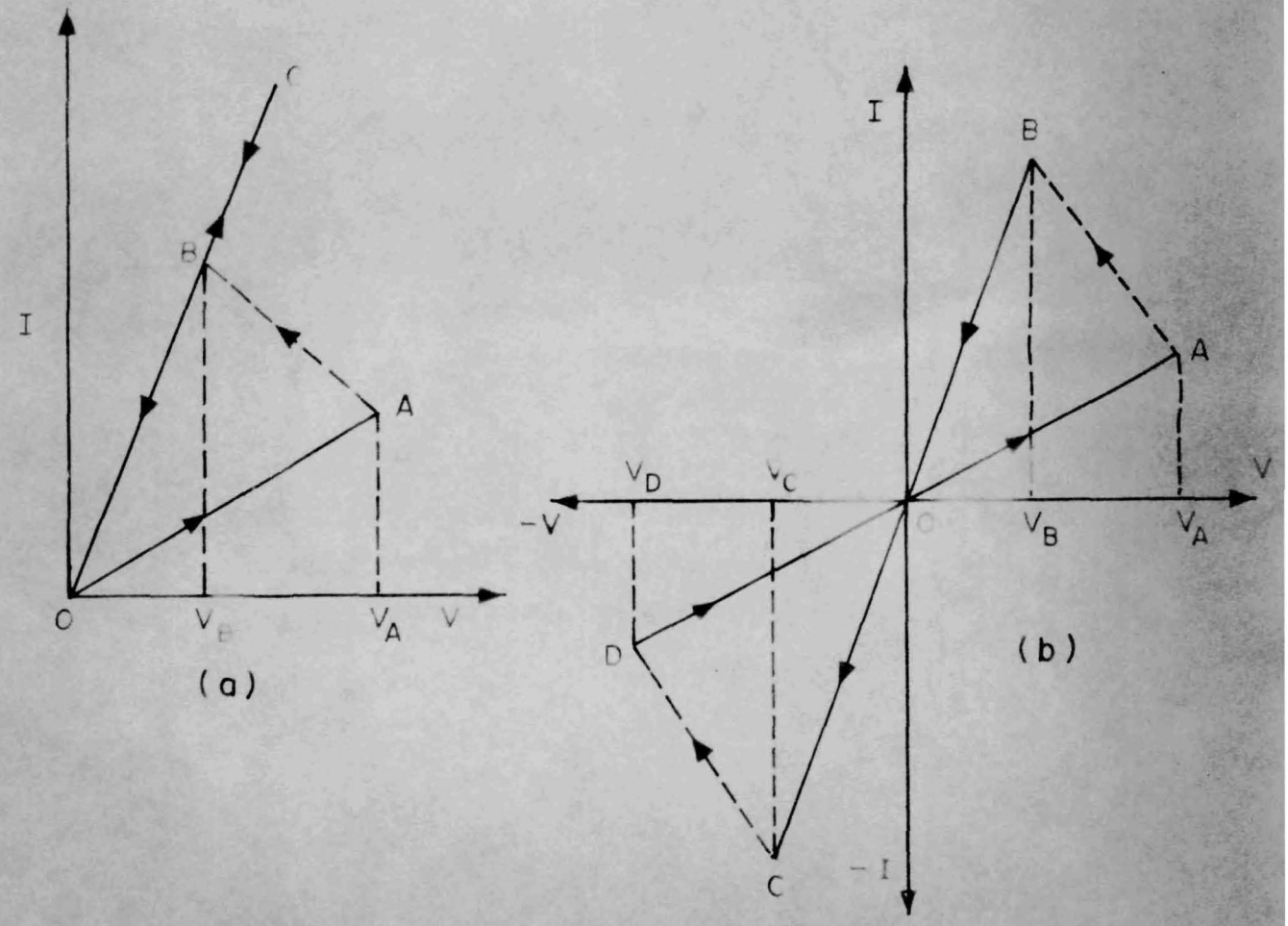


FIG. 1.11 BISTABLE STATE WITH SWITCHING
(a) WITHOUT MEMORY; (b) WITH MEMORY.

to one in Fig. 1.11a i.e. OABCBOA ... then the sample would be said to be bistable and to show "switching" between the state OA and OB. Here the negative resistance part AB is not reversible and on decreasing the voltage a new path CBO and not CBAO is followed. The sample, in other words, switches from the state OA to OB at the voltage V_A and vice versa, at VO. This type of sample does not have "memory" because on switching the voltage off (i.e. V = 0), it would be having the resistance corresponding to OA whether we came to O from a point on OC or OA.

The sample would be said to be "bistable", to show "switching" and to have a "memory" when the curve shown in the Fig. 1.11b is followed. Here the I-V path is OABOCDOA ... It can be seen that the part OABO is similar to that in Fig. 1.11a and also switching from OA to OB takes place at V_A in the same manner. However, the switching back from the state OB to OA does not take place at V = 0, but at a reverse voltage of V_C. Thus at V = 0, the sample can be either in the state COB or DOA depending on its past history (i.e. the magnitude and direction of the applied voltage). This effect would be called "memory".

In what follows we give a brief account of above cited phenomena with particular references to metal-insulator-metal sandwich structures.

1.5.i CURRENT CONTROLLED NEGATIVE RESISTANCE

CCNR can be described as follows : On increasing voltage, current rises steadily up to certain voltage and then it increases suddenly with a simultaneous drop of voltage. After a certain minimum in voltage, the current rises again with voltage. Fig. 1.10a shows the general behaviour of this phenomenon. This behaviour in the I-V characteristic is reported frequently but not yet fully understood. There are a number of proposed theories based on different mechanisms. The important ones are discussed below.

(a) Avalanche injection

The theory of negative resistance based on avalanche injection has been developed by Gunn[37]. The carrier energy increases with voltage and at a threshold voltage V_t, the carrier multiplication takes place giving a sudden increase in current. Additional ionised carriers set a space charge which produces a considerably large field near the anode. A further increase in the current results in limiting the field to a very thin

region near the anode while the field in the entire region is nearly reduced to zero. The avalanche region becomes a source of holes and one can draw more current at low field.

Chopra[38] has observed a similar CCNR in Nb-oxide thin films. Current first rises linearly, then exponentially and at higher voltage a sudden breakdown occurs. He observed that with a decrease in temperature the breakdown voltage increases while the current density decreases. At low temperature, in prenegative resistance state, the current obeys V^2 dependence and after the negative resistance the current obeys the law :

$$I = I_0 e^{\alpha \sqrt{V}}$$

which is similar to Townsend discharge equation. He has concluded that the phenomenon is a bulk property.

He[39] has also reported a similar negative resistance in thin CdS film sandwiched between Au electrodes. To start with, the I-V characteristic is linear with a low impedance which subsequently changes to asymmetric rectifier-like behaviour of a considerably higher impedance. On increase of voltage CCNR appears first on the blocking side and later on both sides. He was not able to explain

the existence of the low impedance ohmic state of the virgin sample. CCNR phenomenon has been explained on the basis of impact ionisation of traps or impurities leading to avalanche carrier multiplication. The mechanism of avalanche breakdown has also been used by him[40] to explain the CCNR in thin oxide films of Ta, Nb and Ti. He has proposed that the space charge set up by the slow moving holes redistributes itself in such a way that it gets concentrated in a thin critical region capable of maintaining the avalanche. This explains the negative resistance in the 'reverse' direction of the rectifying structure.

(b) Double injection with change in lifetime

Lampert[14] has suggested a mechanism for CCNR on the basis of double injection. He has assumed that the insulator contains acceptor-like levels which lie below the Fermi level and for which $\sigma_p \gg \sigma_n$ (σ = capture cross section). At a certain voltage V_{th}, hole lifetime increases and injection starts. Then the current increases and the voltage drops to :

$$V_s = (\sigma_n/\sigma_p)V_{th}$$

(V_s sustaining voltage) giving the CCNR. The presence of traps gives rise to sensitivity to light and hysteresis in the I-V curve.

Geppert[41] observed a symmetrical CCNR in Nb-Nb oxide-Me structures which he also has attributed to double injection with unequal lifetime of electrons and holes.

Hening[42] has reported N- and S- type negative resistance and relaxation oscillations in Au-doped double injection Ge diodes. VCNR (N-type) has been observed below 65° K, before the CCNR (S-type) with double injection becomes important. N-type negative resistance has been explained by an occupation of the 0.2 ev gold level, while the generation of oscillations has been related to the S-type negative resistance.

(c) Avalanche breakdown double injection

Steel et al[43] have studied the I-V characteristic of forward biased p-n junction. They have concluded that the injection of minority carriers in the body of the diode is essential for the breakdown. According to them the negative resistance is due to current that follows the onset of avalanche breakdown at the point contact.

Beam and Armstrong[44] have proposed a mechanism where an impact ionization of the metal ions is caused by the carrier injected into the oxide by Schottky field emission or tunneling.

Ridley[45] has invoked high current filament formation to explain the current controlled negative resistance and formation of high field domains in the case of VCNR.

Van Heck[46] observed current saturation and negative resistance in evaporated CdSe thin films which have been explained as due to trapping of hot charge carriers at the repulsive centers in the grain boundaries.

1.5.ii VOLTAGE CONTROLLED NEGATIVE RESISTANCE

Voltage controlled negative resistance can be described as follows :

The current first rises steadily with voltage upto a critical value beyond which an increase in voltage reduces the current. After a certain minimum value, current again rises steadily with voltage.

Kromer[47] has proposed a mechanism on the basis of the fact that the high kinetic energy electrons and

holes in semiconductor have negative masses. The contribution due to these carriers will show a negative effect.

Ridley and Watkins[48] have suggested that the carriers at high electric fields can be transferred into sub-bands higher in conduction band, where mobility is low due to large effective mass in the band. Decay in mobility will give rise to voltage controlled negative resistance.

Ridley and Watkins[49] have also shown that the steady state density of the conduction electrons falls at higher fields due to the increased rate of capture of electrons by the repulsive centers, which leads to the VCNR phenomenon.

Ridley and Pratt[50] have reported bulk negative resistance in gold doped germanium and have contributed it to the formation of high field domains within the bulk of the semiconductor. Formation of these domains is explained on the basis of electron tunneling through the repulsive trap centers whose capture cross section increases with field.

Hickmott[51] has observed VCNR in Al-Al oxide-Al sandwiches and has explained the results on the basis of positive dipole formation caused by the field ionization of metal donors in non-stoichiometric film, which increases the barrier.

Pollack et al[52] have studied the vapour deposited films of Al-oxide sandwiched between two metal electrodes. After a complete formation of ionic space charge layer, the phenomenon of VCNR is observed.

Hickmott[53] has also studied the negative resistance in anodic oxide films and explained it as due to the formation of impurity band close to the Fermi level which initially helps in tunneling of electrons from metal to metal through traps. The transfer of electrons to the conduction band from the other levels or valence band increases exponentially with field. This reduces the tunnel current at higher fields across the sample and so VCNR is observed.

VCNR has also been observed by Epshtein[54], Ioffe[55] and Pemidenkov et al[56] and has been attributed to the electron-phonon interaction. Bonch[57], Ihanova et al[58] and Boer[59] have given the theory of domain formation to explain the acousto-electric instabilities.

Mead and Spitzer[60,61] reported voltage controlled negative resistance of one polarity and explained it on the basis of the Fermi level position at the metal-semiconductor contact.

1.5.iii BISTABLE CONDUCTIVITY WITH SWITCHING AND MEMORY PHENOMENA

McWhorter and Rediker[62] (1959) reported "switching" in doped germanium at liquid He temperature due to avalanche breakdown produced by impact ionisation of III or V group impurities. The ionisation switches the sample from high to low impedance state. Switching back occurs when the carriers recombine with ionized impurities. This device was named "cryosar". They discussed two types of cryosars, one using uncompensated Ge which has high impedance ($\sim 10^7$ ohm cm.) till a critical voltage where current increases by more than seven orders of magnitude: and the other utilising a compensated p-type Ge. This one exhibits a similar electric characteristic except that a negative resistance occurs between the low and high impedance states. This is a "bulk" behaviour since both contacts are ohmic. Switching time is of the order of 10^{-8} secs.

Kessler and Tompkins[63] (1963) have found that p-type Ge wafers doped with lithium (high atomic mobility,

n-type dopant) could be used for a junction device called "flexode". I-V characteristic of this diode could be reversibly transformed from rectifying state to a resistive one by applying a electric field at elevated temperature (more than 100° C). Transformations are caused by field enhanced diffusion of Li ions. Reverse bias is believed to cause electric field controlled precipitation of excess of Li ions in the p-n junction region. Precipitation degrades the rectifier characteristic and finally rectification disappears since p-n junction is shorted. Former rectifying state is re-established by applying forward bias.

Hiatt and Hickmott[64] (1965) have observed a bistable conductivity in Nb-Nb oxide-metal diodes. If the voltage across Nb-Nb oxide-Bi is slowly raised, a sudden breakdown occurs to a high conductivity state. The original high diode resistance can not be recovered but the diode may be repeatedly switched between high and low conductivity states. The diode after breakdown is in stable high conductivity state which is frequently characterized by CCNR. On reversing the diode polarity, it switches to a low conductivity state which is stable, even if the polarity is changed upto some critical voltage, where diode again switches to the high conductivity state

and cycle could be repeated. In addition, they also reported that CCNR in the same diode may appear at two different voltages. If instead of Bi, In electrode is used a similar electrical behaviour is obtained except that VCNR inflection is also observed in the low conductivity state besides the well-developed CCNR. Contrary to Beam and Armstrong[44] and Chopra[38], Hiatt and Hickmott find that the metal electrodes play an important role because samples with Zn, Cd, Pb and Sn counter electrodes do exhibit both CCNR and VCNR, but those with Au, Ag, Al or Hg do not i.e. there is no observation of VCNR in the low conductivity state. Most pronounced switching is obtained with Bi, In and Pb where it occurs even at low temperatures (4.2^{o} K). They have not been able to give any explanation of this complex behaviour.

Mizushima and coworkers[65] (1965) have reported switching phenomenon accompanied by avalanche breakdown in thin films of semi-insulating GaAs sandwiched between two metal electrodes (W, Mo base and Al, Te as counter electrodes). They have found that metal hardly influences the electrical behaviour. On applying voltage to the sandwich in any direction the sample switches from low to high conductivity state. Turnover voltage is thickness

dependent and for films of 0.01 to several microns, it varies from 1-30 V. Sustaining voltage is nearly constant (0.7 to 1 V). Temperature effect is almost negligible in the range of 77^{o} K - 450^{o} K. Switching time is estimated to be less than 10 ns. In their next paper[66] they have investigated the thickness dependence of breakdown, turnover and sustaining voltages. Breakdown voltage is that voltage where formation takes place. Switching appears at somewhat lower voltage. The breakdown voltage is nearly proportional to the thickness, while the behaviour of the sustaining voltage is abnormal i.e. it does not depend on thickness, which is in marked contrast to "cryosar". Sustaining voltage seems to consist of an injection voltage (0.65 V) and a sustaining voltage (5×10^{3} V/cm, by thickness d). Temperature does not have any detectable effect on V_b, V_t and V_s. They ruled out avalanche injection mechanism in the region of the sustaining voltage since this voltage deduced from Gunn[37] theory and current multiplication measurements in the pre-breakdown state never comes less than 1 V. Their sustaining voltage is about a half of the band gap energy (GaAs Eg. 1.4 ev).

Takagi and Mizushima[67] (1967) have observed negative resistance and switching accompanied with breakdown

in single crystal films of CdS grown by sublimation. Deposited In and Au plated Mo wire have been used as contacts. Crystals have been examined by applying pulse field of 2 micro sec. width and 30 Hz repetition frequency. Current is very small under low field since the sample resistivity is about 10^6 ohm cm. On increasing the field, current slowly rises and at a certain critical voltage, a sudden rise of current takes place. When the applied pulse amplitude reaches the turnover voltage, the current rises rapidly and the terminal voltage drops simultaneously. Switching characteristic is independent of the choice of polarity of the applied voltage. They have also found that the breakdown voltage is proportional to the sample thickness. Turnover voltage is unstable and decreases after repeated operations. The sustaining voltage has been observed in the same fashion as in the previous work on GaAs[65,66] i.e. composed of the two parts, one injection voltage independent of the thickness and second a thickness dependent voltage. On the basis that sustaining voltage in CdS is somewhat higher than that in GaAs, they have included the possibility of avalanche injection contribution to yield the negative resistance and to sustain the discharge state. The authors have ruled out double injection mechanism on the basis of the fact that very little temperature effect has been observed on these critical voltages.

The sample shows good photoconductivity before breakdown, but is insensitive to light in the switching state.

Patil and Sinha[68] (1967) have reported an unusual negative resistance phenomenon in evaporated CdS thin film sandwiched between two Al electrodes. After breakdown at a certain critical voltage CCNR is followed by VCNR when the polarity of the bias is changed. Initially, the sample has high resistance and current is small under moderate applied electric field. At a certain voltage current rises suddenly. This transition takes place when bottom Al electrode is made negative. On reducing the voltage, the sample remains in the high conductivity state. Only by changing the bias polarity, sample switches from high conductivity state to the former low one. Cycle can be repeated if bias polarity is again changed making bottom Al electrode negative. As the initial high impedance state of the virgin sample can not be re-established, the first switching is defined as breakdown. They have also found that temperature has only a little effect on the switching voltage but not at all on sustaining voltage. Furthermore, thickness as well as electrode material do not have any significant effect on the sustaining voltage which in their studies appears to be about 1.7 V.

Sakamoto[69] (1967) in his studies on electro-luminescent properties of thin ZnS evaporated films, doped with Pb, Cu, Cl has observed a similar behaviour in steady state I-V characteristic. He has found that at some critical applied voltage, current suddenly rises. The sample remains in this state unless the sign of voltage is changed, when it switches to the low conductivity state. No explanation has been given.

One of the most detailed presentation on the switching phenomena has been reported by Simmons and Verderber[70] (1967). They have observed negative resistance, switching and reversible memory effects in thin evaporated Si-oxide films sandwiched between Au and Al deposited electrodes. Film thickness ranges between 200-300 $\mathring{A}$. The observed electrical properties have been attributed to result from electrolytic introduction of Au ions from gold electrode into the SiO film. The sample shows temperature independent conductivity, voltage-controlled negative resistance and reversible voltage and thermal-voltage memory effects. The formation process has been related to the introduction of Au ions which takes place under a certain voltage applied on the sample placed under a moderate vacuum. To develop formation it is necessary to make Au electrode positive. After this process, the

sample which initially has a high impedance turns over to a low impedance state. Current through a formed sample is eight orders of magnitude higher than that of the unformed one. If voltage is slowly reduced to zero a pronounced VCNR region is observed. Any repeated D-C voltage sweep produces the same characteristic, thus the change in conductivity is permanent. In view of the facts that (i) Al-SiO-Al sandwiches do not show a similar behaviour, (ii) it is necessary to make Au electrode positive to get the formation, and (iii) the formation can not take place at temperature lower than - 50° C, it has been concluded that formation is due to the injection of Au ions. In fact, the formation occurs more readily at an elevated temperature. On reversing the bias polarity at high voltage, the sample may revert to high impedance state which suggests that ions are swept out from the insulator.

I-V characteristic of the unformed sample shows $\log I \sim V^{1/2}$. A strong temperature dependence[71] of current is also observed. After formation, the current rises steadily with voltage and at $V \sim 4$ v negative resistance region appears. On decreasing the voltage the curve is more or less retraced. Peak to valley ratio

is 100:1. The voltage at which peak current occurs is thickness independent. D-C characteristic is very stable upto 2.5 v which is designated as threshold voltage (V_{th}).

On the other hand, after going through the negative resistance, if the applied voltage is reduced to zero in less than 0.1 ms., the original curve is not retraced and the sample remains in a high resistance state. To come back to the conducting state, a voltage in the opposite direction has to be applied. However, this behaviour is symmetrical in the sense that any direction of applied voltage beyond the threshold would induce the high resistance state which would be erased by a voltage of opposite polarity.

Negative resistance has been explained on the basis of the formation of a narrow band in the forbidden gap. At low voltages, conduction takes place through this band, but at higher voltages this is suppressed below the Fermi level in the metal and is therefore not available for conduction. This causes a sudden decrease in conductivity and hence a negative resistance. The memory is attributed to some trapped charge stored in the semiconductor, when the voltage is released quickly. The stored charge distorts the band structure of the insulator

such that the resistance increases. The stored charge is withdrawn on the application of voltage of opposite polarity and the original conduction restored.

Argall[72] (1968) has reported reversible switching from high impedance to low impedance state in Ti-oxide thin films.

Films have been fabricated by anodization of Ti metal sheets in an electrolyte. Vacuum deposited Al, Au, Ti and Bi have been used as counter electrodes. Film thickness is about 100 Å. I-V characteristics have been traced on an oscilloscope by applying 100 Hz signal. Initially, the I-V characteristic of the insulating state is slightly asymmetric. However, just before breakdown, marked change occurs followed by uncontrolled switching. This transition is fairly complex, it can be accompanied by CCNR or it may even switch to a high conductivity ohmic state. Besides that, these transformations follow each other in a fairly random order but one can distinguish controlled switching between high impedance and low impedance states. He has found that there is no need for special environments and the transitions take place either in vacuum or in air in the temperature range of 77-500° K. Switching can be

obtainedeither by voltage cycling or by applying pulses. Several switching cycles may cause failure i.e. sample may remain either in the low or high conductivity state (10 ohm). The author does not find that electrode material plays any decisive role. There is no observation of VCNR even in the sample placed under vacuum and having Au electrode, contrary to that found by Hickmott[51] for thin anodic oxides and by Simmons and Verderber[70] for Si-oxide. Argall finds that current in any state is proportional to the contact area and thus the bulk of the dielectric is active. Furthermore, it has been noticed that each conducting state has its own I-V characteristic, activation energy or lack of it.

At 77° K, before switching is established, I-V behaviour is ohmic at low voltages, followed by a square law region and finally by a region where $I \sim V^6$. After switching the state is characterized by $I \sim V^{3/2}$. Third state is pure ohmic. These three states are asymmetric with respect to voltage and exhibit memory. When switched off in a particular state the film remains in the state without any change. Square law region of the I-V characteristic of the state (1) is attributed to SCL mechanism as proposed by Lampert[73] and the higher power region of $I \sim V^6$ due to some form of space charge limited

conditions, the three-halves power law of state, (ii) to filamentary injection and ohmic region of state, (iii) to some form of electron hopping conduction. The author has not proposed any theory to explain the switching mechanism. He merely rules out the possibility of a phase change because the dielectric constant remains unchanged throughout the switching action.

Feldman and Gutierrez[74] (1968) have observed CCNR and switching in amorphous boron films deposited from boron by electron bombardment. Vacuum deposited titanium has been used for both electrodes. On applying voltage, current is first proportional to V then to V^2 and finally to V^n where n is greater than 3. Further increase of current in this state leads to an irreversible breakdown. Former space-charge region $I \sim V^2$ is not found after breakdown. Switching is possible in this formed state. Threshold voltage where CCNR occurs and sustaining voltage are independent of sample thickness, the ratio of V_{th}/V_s is equal to the ratio Eg/Er, where Eg is the band gap and Er is the energy of the recombination level.

Furthermore, temperature does not influence the threshold and sustaining voltage. They propose a model

based on a change in electron capture cross section due to filling of recombination level with electrons by avalanche ionization.

The authors used the model given by Lampert[14] and Stafeev[75] invoking the role of recombination level in the switching mechanism. In addition, they postulate the mechanism of filling the level. It is assumed that the starting material is p-type with recombination level in the middle of the band gap. Recombination centers are filled with holes and are thus able to capture electrons from the conduction band. The hole current is first ohmic, then space-charge limited until the avalanche threshold voltage is reached where holes are ionized to valence band. V^n dependence results from the increased hole current. On increasing voltage further, electrons are ionized to the conduction band, where they have a long lifetime. Current is now carried by both holes and electrons. Transit time does not come in picture due to the thinness of the sample, hence the behaviour is thickness independent. Resistance drops until the voltage across the sample is just sufficient to keep the recombination centers free of holes by ionization. By reversing the cycle, the recombination centers begin

to fill with holes, the electrons are captured and the resistance increases. The sample then turns to the original state.

Ovshinsky[76] (1968) has reported reversible switching phenomena in disordered structures e.g. amorphous semiconductors like oxide, boron-based glasses and materials containing As or Te combined with others from III, IV and VI group. It has been concluded through field effect measurements that band gap contains a distribution of trapping and recombination centers with densities in excess of 10^{19} cm^{-3} eV^{-1}.

The major features of the switching phenomenon are the following : I-V characteristic is symmetrical with respect to the reversal of the applied voltage and current. The methods of the sample preparation and electrode material do not play any role. Highly resistive state is ohmic at fields below 10^4 v/cm. At higher fields dynamic resistance decreases monotonically. When applied field exceeds a threshold value, the sample switches to the conducting state. In the conducting state the current can be increased or decreased without affecting the voltage drop, this voltage is termed as the holding voltage V_h. Here the dynamic resistance is close to zero. If the

current is reduced below the characteristic value, termed as holding current I_h, the sample switches back to original highly resistive state. The switching process is repeatable. In the high resistive state the threshold voltage increases almost linearly with the thickness of the sample. On this basis and on the unimportance of the electrode material, it is concluded that the current in the high resistive state is bulk limited. In contrast to this the holding voltage is weakly dependent on thickness which suggests that in the conducting state the voltage drops entirely at one of the electrodes. On switching to the conducting state, current filaments appear to form which grow with increasing current flow. Similar current filaments have been observed by Boer[77] and coworkers and are quite generally associated with 'S' shape instabilities. By applying rectangular voltage pulses it has been found that switching occurs with a delay time t_d. The duration of switching process is less than 1.5×10^{-10} sec.

The switching process can be analysed in terms of the nucleation theory where nucleation rate is voltage dependent. The conduction and switching processes are closely related to the structural disorder and the amorphous nature of the materials which in turn are

associated with the local bonding characteristics of the constituent elements. The disorder allows most atoms to complete their valence state and thus establish a high degree of compensation resulting in insulating behaviour of these materials. A large overlap in energy of the levels stemming from the valence band with those from conduction band is expected to produce a large density of traps. These traps when they are occupied can easily be ionized at moderate fields by lowering the trap depth and reducing the capture cross-section[78]. Rapid increase of carrier concentration results and can explain the observed non-ohmic behaviour in the low conductivity state. Exponential dependence of current on voltage in high resistive state, before switching is explained as internal field ionization and emission from localized states. It is believed that after switching a re-distribution of carriers, as a result of oppositely charged carriers having very different mobilities and transition rates through the electrode interfaces, gives rise to a space charge and field enhancement near one electrode and to the small value of V_h.

A memory effect has also been observed. After switching from high resistance state, structural changes

result in the preservation of the conducting state even when the voltage is removed. The material can be reversibly switched back to the high resistance state by application of a current pulse of either polarity exceeding a threshold value.

In what follows we report a new type of bistable conductivity, switching and memory effect in thin films of CdSe and CdTe sandwiched between two metal electrodes.*

---

* A short note describing these effects has already been published[79] (1968).

1.6 SOME PROPERTIES OF CADMIUM SELENIDE AND CADMIUM TELLURIDE

CdSe and CdTe are semiconductor materials which first attracted attention because of their photoconductive and luminescent properties. Although these two materials have been studied considerably less than the other compounds of II-VI class such as CdSe and ZnS, there is still a vast amount of publications on the study of these two compounds.

1.6.i. CRYSTAL STRUCTURE

CdSe and CdTe usually crystallise either in zincblende or hexagonal-wurtzite structures depending on the stoichiometry and preparation conditions. In addition, some polytypes are also known to exist.

The zincblende structure (ZnS) is based on the cubic space group T_d^2-$F\bar{4}3m$. There are four ZnS molecules in a unit cell. The atoms occupy positions with the following coordinates : 4S in (a) 0,0,0; 0,1/2,1/2; 1/2,0,1/2; 1/2,1/2,0 and 4Zn in (c) 1/4,1/4,1/4; 1/4,3/4,3/4; 3/4,1/4,3/4;3/4,3/4,1/4. Every atom is surrounded tetrahedrally by four atoms of the other kind at a distance of $\frac{1}{4}\sqrt{3}$ a where 'a' is the cubic lattice parameter. There are twelve next nearest neighbours of atoms of the same kind at the distance $\frac{1}{2}\sqrt{2}$ a.

Six of these are distributed at the corners of a hexagon in the same plane as the central atom; the remaining six form a trigonal antiprism with three above and three below the plane of the hexagon. Zincblende arrangement does not have a center of symmetry or inversion. The zincblende crystals are polar and the opposite faces e.g. (hkl) and $(\bar{h}\bar{k}\bar{l})$, and opposite directions $[hkl]$ and $[\bar{h}\bar{k}\bar{l}]$ may have different physical and chemical properties (Fig. 1.12).

The wurtzite structure (ZnS) has the space group C_{6v}^4-$P6_3mc$ and there are two molecules in the hexagonal unit cell with two Zn at 0,0,0; 1/3,2/3,1/2 and two S at 0,0,u; 1/3,2/3,$\frac{1}{2}$ + u with u $\sim$ 3/8. Each Zn atom is bonded to four S atoms, approximately at the corners of a tetrahedron, one at the distance 'uc' and three at $\left[\frac{1}{3}a^2 + c^2(u-1/2)^2\right]^{1/2}$. There are twelve nearest neighbours: six at the corners of a hexagon in the same plane as the central atom at the distance 'a'; the remaining six are at the corners of a trigonal prism at the distance $\left[\frac{1}{3}a^2 + \frac{1}{4}c^2\right]^{1/2}$. If $c/a = 2\sqrt{2/3} = 1.6330$, and if u = 3/8, the nearest-neighbour coordination is tetrahedral and the twelve next nearest-neighbour distances are equal.

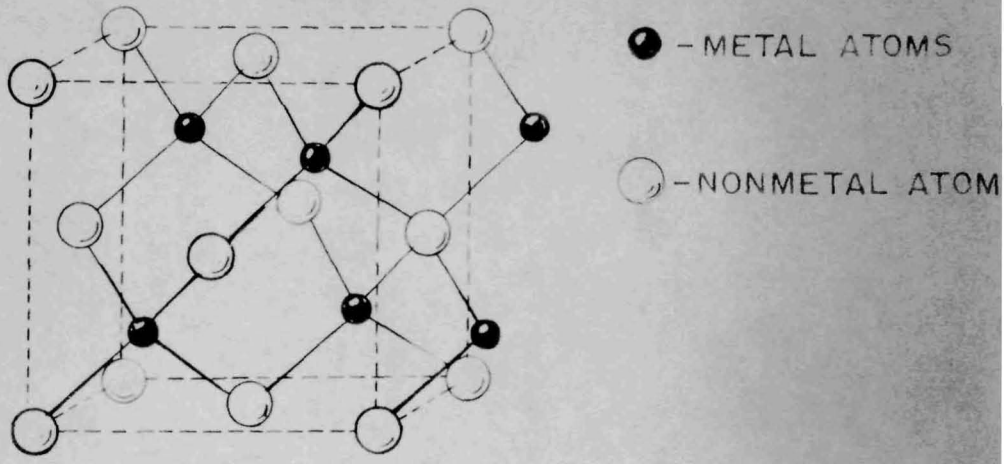


FIG. 1.12 ZINCBLENDE STRUCTURE OF THE CUBIC ZnS (*Pauling*)[80]

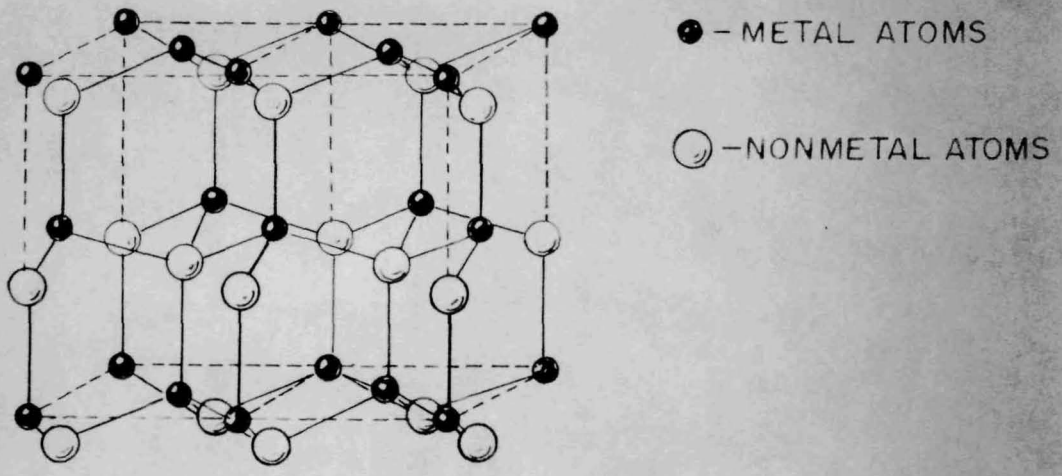


FIG. 1.13 WURTZITE STRUCTURE OF THE HEXAGONAL ZnS (*Pauling*).[80]

Wurtzite does not have a center of symmetry and there is a polar axis parallel to [0001] (Fig. 1.13).

(a) Cadmium selenide

Both zincblende and wurtzite forms are known. For the zincblende form the lattice parameters are : a = 6.05 Å ; d_{Cd-Se} = 2.62 Å; d_{Cd-Cd} = 4.28 Å while for the wurtzite form they are : a = 4.2985 Å; c = 7.0150 Å.

(b) Cadmium telluride

CdTe usually crystallizes in the cubic zincblende arrangement, with the lattice parameters : a = 6.481 Å ; d_{Cd-Te} = 2.80 Å and d_{Cd-Cd} = 4.58 Å , although sometimes the wurtzite type has also been reported. Hexagonal cell dimensions extrapolated from the lattice parameters obtained from hexagonal solid solution Cd(Se, Te) are a = 4.57 Å and c = 4.58 Å .

1.6.ii ELECTRICAL PROPERTIES

Electrical properties of the CdSe have been studied less extensively than those of CdTe mainly because it is difficult to prepare CdSe single crystals of high purity. CdSe and CdTe have the band gap of 1.7 and 1.4 - 1.5eV respectively and the fundamental absorption edge lies in

the near infrared. Electron effective mass m^*/m in CdSe is about 0.13 and mobility around 500 $cm^2/v.sec.$ determined at room temperature for an n-type material having the carrier concentration of the order of 10^{-17} cm^{-3}.

CdTe is unique* among II-VI compounds in the sense that it can be made either n-type or p-type. Effective mass (m^*/m) is about 0.13 for electrons and 0.41 for holes. However the experimental value of m^*/m has been found to depend on the method of determination. Activation energy is about 0.003 eV for an n-type CdTe and 0.3 - 0.5 eV for p-type. Large activation energy for p-type CdTe shows why so far there has been difficulty in getting p-type conductivity in II-VI compounds. Jenny and Bube[82] have reported that n-type conductivity in CdTe is obtained with impurities from III or VII group and p-type from I or V group. Au, Cu and Ag diffuse extremely rapidly in both materials as interstitials but they can also substitute Cd in the lattice. Ga and In act as donors by substituting Cd. Jenny and Bube[82] have determined

---

* It is worthwhile mentioning that recently successful preparation of p-type CdSe single crystal has been reported[81].

carrier mobility as 30 cm^2/v sec. for both p-type and n-type material by Hall effect measurements. Oxygen as an impurity in II-VI compounds plays a very important but rather a complex role. Its presence in these materials may lead (i) to the formation of solid solutions between the chalcogenide and oxide producing a shift in the pertinent energy parameters (ii) to the appearance of specific discrete levels or bands within the forbidden gap, and (iii) to certain surface phenomena. Normal adsorption, thermal desorption as well as photostimulated adsorption and desorption have been observed. The last one has been studied in great detail by Bube and coworkers[83,84,85]. In general oxygen acts as acceptor-like impurity, it decreases dark conductivity in the CdSe but increases the ratio I_l/I_d. Most of the past treatments in fabricating photosensitive elements are related to oxygen adsorption.

Brodie and LaCombe[86] have found the dielectric constant of CdSe as 9 at 4.2° K, 9.5 at 77° K and 10 at 240° K. For CdTe, DeNobel[87] has reported the dielectric constant as 10.9 at 20° K and 11.0 at 77° K, measured on p-type material with the carrier concentration of $5.5 \times 10^{13}/cm^3$.

1.6.iii. CdSe AND CdTe AS THIN SEMICONDUCTOR FILMS

Many of the important solid state phenomena such as photovoltage, photoconductivity, storage and electroluminescence have been found in thin layers of these two materials or in their solid solutions with other materials of the II-VI group. These films are already used in some devices such as field effect transistors and photoelements and some are under further investigations. There are a number of ways of preparing thin films of these materials such as chemical deposition, sublimation, sputtering, vacuum evaporation, epitaxial growth and so on. Depending on the way and conditions of the preparation, thin film may appear as a "single crystal" polycrystalline film with preferred orientation of microcrystallites, polycrystalline film of randomly oriented small crystals or amorphous films. As regards to the samples prepared by vacuum deposition, the properties may be affected by many preparation parameters such as purity, physical form of the deposit, deposition rate, film thickness, temperature of the evaporator, geometry of the deposition arrangement, nature of the residual atmosphere, nature and temperature of the substrate and various postdeposition processing. Because of all these and the fact that II-VI compounds

dissociate in vapour phase which causes non-stoichiometry in the deposits there is a fairly poor reproducibility of the observed characteristics of deposited II-VI compounds.

As already mentioned both CdSe as well as CdTe may exist in two crystal modifications viz. cubic zincblende and hexagonal wurtzite forms. Shalimova[88] has found that CdTe sublimed in argon on the glass substrate contains the hexagonal modification (wurtzite type), in addition to the usual cubic form. She has found that the former occurs when the film has an excess of metal. Excess of Te stabilises the cubic form. Thin films sublimed under vacuum do not have the hexagonal form. Large proportion of the hexagonal form occurs when film is deposited at substrates temperature of 70-400° C and evaporation temperature of 500-800° C. The films tend to have the (111) planes of the crystals parallel to the substrates. This texture is lost at low temperature and in the thicker films. The lattice parameters of the hexagonal form are $a = 4.58\ \mathring{A}$; $c = 7.50\ \mathring{A}$; $c/a = 1.637$.

Palatnik and Sorokin[89] have found that anomalous photo e.m.f. in thin evaporated CdTe films is due to a large number of series connected photocells. The photo-effect in each cell is generated at the boundary between

hexagonal and cubic lattices. They[90,91] have concluded that large PEMF can be reproduced only when the substrate temperature is high since only at higher temperature hexagonal form is obtained. Films deposited on white sapfhire substrate has a higher PEMF because Al_2O_3 promotes preferential growth and orientation of the crystallites and blocks of the hexagonal modification[92].

Matsuno and Inoue[93] have studied crystal growth and orientation of evaporated CdTe thin films. p-type CdTe has been deposited on hot substrates (120-250° C) at normal and oblique-incidence (45°). They have found that substrate temperature has a pronounced influence on the orientation of the films. Films consist of fibrous crystallites of size less than 0.4 - 0.8 microns, which show well-defined crystal planes of a hexagonal crystal habit. Strong dependence of growth orientation on the direction of deposition has been proved too.

Piezoelectric effect observed in films grown on quartz, has shown that the Cd(111) plane is adjacent to the substrate. This has been found to hold for most other substrates examined. Photovoltage is higher when the illumination is parallel to obliquely deposited film. Films deposited with normal incidence do note exhibit

photovoltaic effect. The positive voltage develops on the side close to the evaporator. Following Semiletov [90] and Novik[94] the anomalous photovoltage is attributed to a transition structure between cubic and hexagonal phase. Furthermore, it is shown that the lamellae structure perpendicular to [111] axis is introduced during growth. The existence of both hexagonal and cubic phase indicates that lamellae are probably composed by stacking these two phases and the interfaces may be responsible for the photovoltage. Each fiber crystallite plays a role of photovoltaic element and its sign is negative on the substrate side and positive on upper surface side in the case of quartz substrate.

Somarjai[95] has studied interaction of O_2 with CdSe film deposited in the temperature range of 0-360° C and pressure range of 10^{-4} - 10 mm. O_2 decreases dark conductivity of n-type CdSe and thus acts as acceptor impurity. He has also found donor type weakly adsorbed O_2 present on CdSe films which could be reversibly removed from the surface. X-ray shows that deposited film has a highly oriented hexagonal structure with the 'c' axis normal to the substrates. It has been found that vacuum baking containing either large excess of Cd or Se improves

stoichiometry of the compound. Furthermore, they have observed that fast electron transfer from the semiconductor film to the oxygen takes place at any temperature when O_2 is introduced into reaction vessel. This is interpreted as the formation of chemisorbed O_2 of the acceptor type in the monolayer of adsorbed atoms. At high temperature, above 630° C, fast desorbtion takes place and the resistance approaches the value of a "clean" surface. CdSe films remain n-type throughout the experiment.

Shimizu[96] has studied electrical properties of CdSe evaporated films and has found that there are two kinds of electron traps : shallow (0.13 eV) which are responsible for high conductivity in films deposited on the substrate at 100° C and deep traps (0.4 eV) present in films deposited on the substrates at temperature above 150° C.

Brodie and Reed[97] have used a specially developed experimental technique for the study of trapping levels in thin evaporated films of CdSe and found shallow levels near 0.018 eV with a trap density of about $10^{15}/cm^3$ determined by field stimulated emission.

High photovoltage effect has often been reported in evaporated thin films of CdTe. Pensak[98] and Goldstein[99] have reported such an anomalous photovoltaic effect and they

have found that it occurs with samples deposited under oblique incidence. Since photovoltage is limited by the band gap of the material (1.45 eV) it has been concluded that films consist of large number of junctions. They have not found any dependence on the electrode material.

Komaschenko and Fedorus[100] have studied the photo-e.m.f. in CdSe obtained after vacuum thermal deposition of Au, Cu, Ag or Pt on its surface. They claim that external photoeffect from the metal to the semiconductor is unimportant and homogeneous p-n junction is not formed. It has been concluded that photo-e.m.f. in CdSe is of barrier-type origin. The barrier photoeffect in Cu-CdSe photocells appears at a heterojunction. A physical barrier layer has also been formed at the contact of CdSe with Ag, Au, Pt.

Swank[101] has studied surface properties of II-VI compounds of cleaved single crystal samples under ultra high vacuum. Six n-type samples of different materials have been found to possess a negative surface charge resulting from acceptor-like states below the Fermi level at the surface. Acceptor levels are near to the Fermi level which is near the conduction band edge in most cases. Metal semiconductor surface barriers have also been studied by Geppert and coworkers[102], Mead[103], Cowley and Sze[104], Spitzer and Mead[105], Goodman[106,107] Dore et al[108] and many others.

. . . . .

CHAPTER - 2

EXPERIMENTAL

Metal/CdSe or CdTe/metal thin film sandwich structures have been used for the study of the mechanism of the observed bistable conductivity phenomena (switching and memory). The sandwiches have been prepared on insulating substrates by the vacuum deposition technique and their electrical properties have been studied. The techniques have been used for the sample preparation and for the measurements of physical properties are as follows :

2.1 GENERAL DESCRIPTION

Substrates

Metal/CdSe or CdTe/metal sandwiches were normally prepared on glass substrates. Glass substrates (Gold Seal microslides, dimensions 7.6 x 2.54 x 0.1 cm) were cleaned in dilute chromic acid and washed thoroughly by rinsing with boiling distilled water. Finally, they were washed with double distilled water, rinsed with isopropyl alcohol and dried under an infrared lamp.

Cadmium selenide and cadmium telluride

All depositions have been done with CdSe and CdTe supplied by Koch and Light Co., purity 99.999 per cent, without any intentional doping.

CHAPTER - 2

EXPERIMENTAL

Metal/CdSe or CdTe/metal thin film sandwich structures have been used for the study of the mechanism of the observed bistable conductivity phenomena (switching and memory). The sandwiches have been prepared on insulating substrates by the vacuum deposition technique and their electrical properties have been studied. The techniques have been used for the sample preparation and for the measurements of physical properties are as follows :

2.1 GENERAL DESCRIPTION

Substrates

Metal/CdSe or CdTe/metal sandwiches were normally prepared on glass substrates. Glass substrates (Gold Seal microslides, dimensions 7.6 x 2.54 x 0.1 cm) were cleaned in dilute chromic acid and washed thoroughly by rinsing with boiling distilled water. Finally, they were washed with double distilled water, rinsed with isopropyl alcohol and dried under an infrared lamp.

Cadmium selenide and cadmium telluride

All depositions have been done with CdSe and CdTe supplied by Koch and Light Co., purity 99.999 per cent, without any intentional doping.

Vacuum deposition unit

A standard vacuum coating unit supplied by M/s. Hind High Vacuum Co. Ltd., Bangalore, has been used. This unit has an oil diffusion pump preceded by a rotary oil pump and the pressure is measured by Pirani and Penning gauges. This unit can produce a low pressure of about 5×10^{-6} Torr. The source to substrate distance could be changed but in order to have maximum reproducibility, the distance was kept constant at about 12 cm. All depositions have been done by resistive heating of a tungsten filament made of a tungsten wire and shaped in proper form.

Mask

For all electrical measurements glass substrates were made by cutting micro slides parallel to the shorter side in 7 small pieces of dimensions of about 2.54 x 1 cm. After masking, these small pieces were carefully laid down on the Mask No. 1 (Fig. 2.1). By this way one can deposit 35 separate samples of above size in one run. Two sets of masks, as shown in Fig. 2.1, were cut out from a mica sheet. The mask was set on a frame which allows place for five microslides.

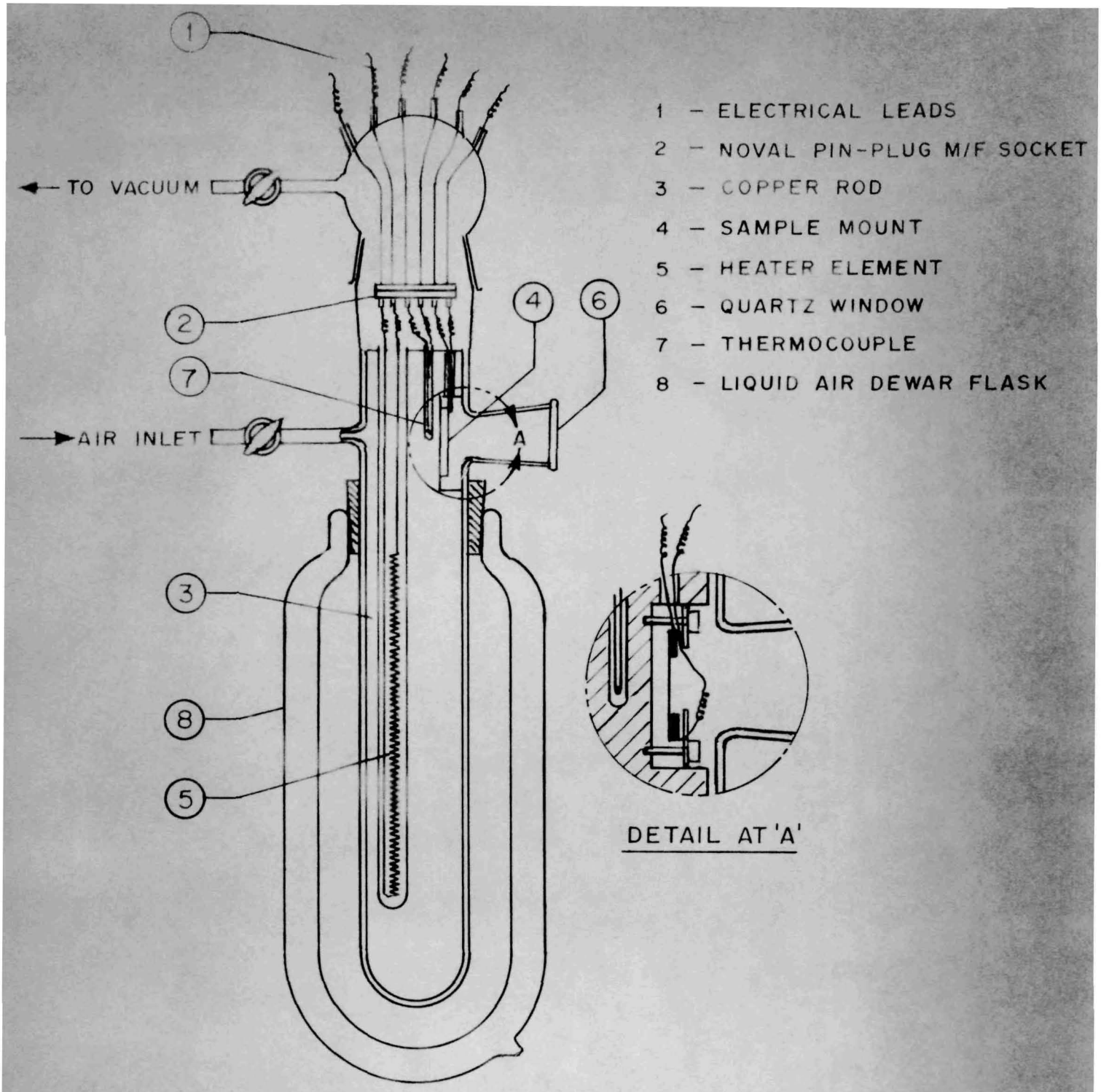


FIG. 2.2. SAMPLE HOLDER ASSEMBLY

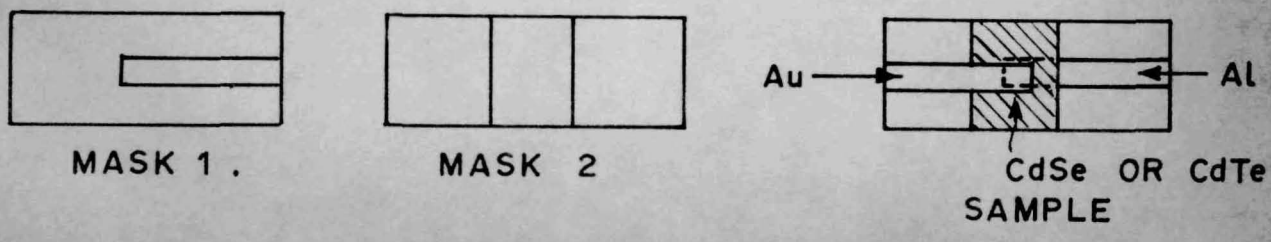


FIG. 2.1. MASKS AND SAMPLE

2.2 PREPARATION OF SAMPLES

CdSe or CdTe sandwiches were prepared with three different electrode combinations as shown below :

Al-CdSe or CdTe-Au

Au-CdSe or CdTe-Au

Au-CdSe or CdTe-Al

Samples were prepared in the following way.

Base electrodes

The glass substrates were put on the frame with Mask No. 1 on top (Fig. 2.1). For deposition of aluminium, filament was made of two tungsten wires (diameter 0.5 mm) twisted and shaped in the form of a coil (0.8 cm. dia.). With such a filament one can carry out many deposits, without possible burning of the filament due to alloying with aluminium since sufficient amount of heat is developed to provide very fast deposition. A tungsten filament which had been flashed earlier was loaded with about 0.05 gr. spec-pure aluminium foil (Johnson and Mathey). Gold was deposited from another tungsten filament. When vacuum of about 5×10^{-6} Torr was developed, glass substrates previously cleaned by ionization under vacuum of about 5×10^{-2} Torr, were heated upto 350° C for half an hour

and then cooled. Substrates were heated by resistance heater made of nichrome wire wound on the mica sheet (10 x 9 cm). The heater was kept at a distance of about 3 cm. above the substrate. Chromel-Alumel thermocouple, whose junction was in close contact with the substrate just below the center of the heater was used for measuring temperature. The temperature gradient was not more than 20° C along the longer side of the mask and 10° C along with shorter side. The substrates were then cooled down to room temperature without breaking the vacuum and the deposition of the metal was started. Time of deposition was kept as short as possible for all metals.

Deposition of CdSe or CdTe

After the deposition of the base electrode, air had to be let into the system to enable us to change the mask for the semiconductor deposition. Both CdSe and CdTe were deposited from silica crucibles placed in a tungsten filament basket. Glass substrates with already deposited base electrode were mounted with Mask No. 2 (Fig. 2.1) on top and the pumping started. When vacuum of 5×10^{-6} Torr. was reached, samples were heated upto the required temperature mentioned below. All these depositions (except when gold was the base electrode

because of the risk of diffusion) have been done on hot substrate temperatures of 150, 200 and 230° C. It was found that the best results were obtained with the samples deposited on the substrate kept at 230° C, so all samples were prepared at this substrate temperature. Temperature of the filament was kept just high enough to provide evaporation (around 700° C). At this rate it took approximately 45 minutes for getting a 1 micron thick deposit. During deposition pressure did not increase above 10^{-5} Torr. After the deposition was over, samples were cooled down to room temperature under the same high vacuum.

Counter electrode

At this state vacuum had to be released again to enable us to change the mask. Samples with already deposited base electrode as well as CdSe or CdTe film were placed on the support with Mask No. 1 on top. Before deposition took place, samples were annealed for half an hour in a vacuum of 5×10^{-6} Torr at the temperature of 230° C. In order to find out the best conditions, a few batches of samples were annealed at much higher temperature, even at 350° C, but no significant differences were observed. After cooling the substrate down to room temperature, the counter electrode deposition was started.

It was found that the rate of metal deposition had to be kept low specially for gold as otherwise the shorting of two electrodes through thin layer of deposited compound occurred.

Electrical leads

For qualitative electrical examinations a pressure contact to the evaporated electrodes was made by placing a silver foil over it and pressing with a crocodile clip. However, for a quantitative electrical measurements, a special unit was constructed in order to carry out the electrical measurements under high vacuum. This unit is described in the next section. In this case, the contact area of both base and counter electrode, was coated with a thin layer of deposited silver since adherence of gold to the glass was very poor. This enabled us to have contacts made by soldering a thin copper wire using Wood's metal solder. Prepared samples were kept in dark under moisture free atmosphere provided by using phosphorus pentoxide traps.

2.3 MEASUREMENTS

2.3.i THICKNESS OF THE FILM

Since we did not have proper facilities for the measurement of film thickness, it was measured by weighing the sample before and after deposition. Thus only the average thickness could be obtained by this method. The thickness dependence of the I-V characteristic has therefore not been studied. In general, the samples had a thickness of 0.5 to 1 micron and an area of cross-section of 0.1 sq.cm.

2.3.ii VACUUM JACKET FOR THE SAMPLE HOLDER

A special unit was constructed in order to measure under vacuum the various electrical and photoelectrical parameters as well as their dependence on temperature (Fig. 2.2). The unit was made of "Pyrex" glass and was painted with black paint. A quartz glass window was built in to enable the illumination of the sample. The unit gets closed by a ground glass joint with eight copper electrical leads sealed in. The unit was also supplied with two stopcocks and one phosphorus pentoxide trap. The longer part of unit, which was not painted was inserted into a thermos flask through a big rubber cork. A thermally insulated funnel was inserted through the rubber

cork for supplying liquid air. Sample holder was made of a chromium plated copper rod of diameter 25 mm. and length 300 mm. Three holes were made along the holder to place a nichrome wire heater and a thermistor or a thermocouple. The sample is placed directly in an appropriately sized depression cut out in the copper body. The unit was connected through a glass vacuum equipment with the Edward's vacuum unit that contains a rotary and a oil diffusion pump. The system was also supplied with Pirani and Penning gauges. This unit enabled any measurements to be taken either in dark or under light and also under a vacuum of the order of 10^{-6} Torr or any other pressure.

2.3.iii. CURRENT VOLTAGE MEASUREMENTS

The various current voltage measurements have been taken for metal/CdSe or CdTe/metal structures in order to ascertain the nature of the current transport. The various details of the methods are described below :

(a) Dynamic characteristic

The sandwich in series with a variable resistance 'R' (see Fig. 2.3) of 0 to 10,000 ohms was connected to a triangular pulse generator 'F'. The voltage drop across

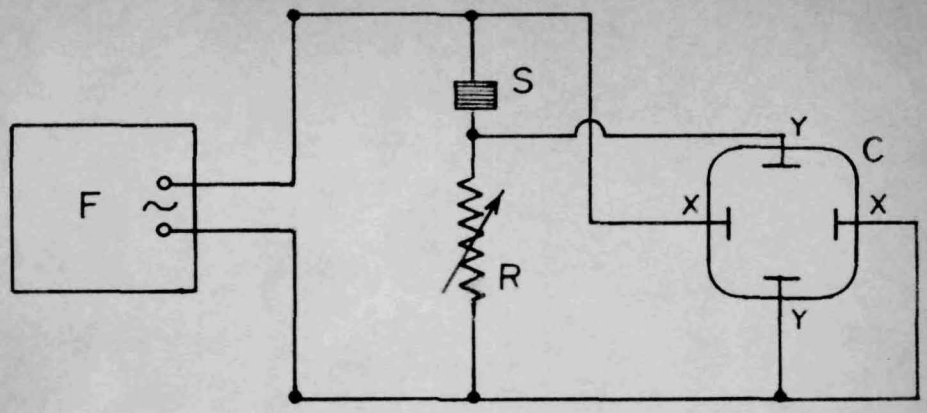


FIG. 2.3. CIRCUIT DIAGRAM FOR DYNAMIC I-V CHARACTERISTICS.

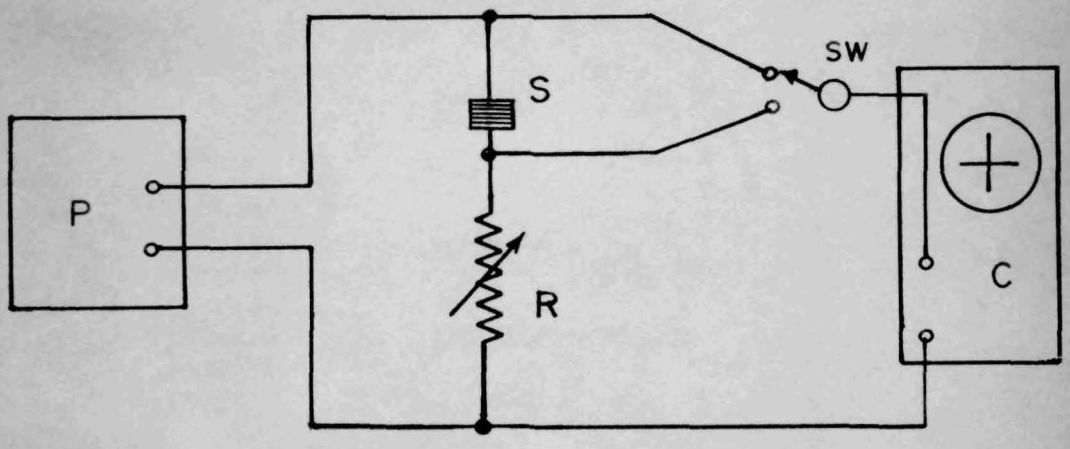


FIG. 2.4. CIRCUIT DIAGRAM FOR PULSE MEASURMENTS.

the sandwich 'S' was led to the X-amplifier while the voltage across the resistance was led to the Y-amplifier of the oscilloscope 'C' (Tektronix 515A). The X- and Y-gain of the amplifier were adjusted so as to limit the trace of the beam within the view of the oscilloscope and was calibrated with the internal calibration signal. As the voltage drop across 'R' was equal to RI (where R is the resistance and I the current) the beam directly traced the current voltage characteristic of the sandwich which was photographed for further analysis. A special care was taken to keep the resistance R small compared to the sample resistance. The range of the triangular voltage V and its repetition frequency was controlled by the control panel of the generator which has an output impedence of 600 ohms and is capable of delivering a maximum current of 12mA at 100 volts with less than 1 per cent distortion. If the generator is loaded, its output voltage falls but still the I-V characteristic of the sandwich remains unaffected. However, for excessive loading the same begins to behave as a constant current generator and current controlled properties of the device can be studied.

(b) Pulse measurements

In order to eliminate the effects of slow states and traps, pulse characteristic of the sandwich was studied.

Fig. 2.4 shows the circuit diagram used for such measurements, where 'P' is a rectangular pulse generator giving pulses of one microsecond duration and repetition frequencies of 1000 c/sec. The current values under pulsed conditions were measured by observing the instantaneous pulse voltage across a resistor 'R' in series with the sandwich 'S' and applied to one of the two 'Y' inputs on the oscilloscope 'C'. The voltage across the sample was measured directly by observing the pulse output on the other 'Y' input on the oscilloscope. The oscilloscope Y inputs could be switched through a switch 'SW' from one to another. Thus both the current and voltage could be recorded separately.

(c) Steady state characteristic

Fig. 2.5 shows the circuit diagram which was used for measuring d.c. I-V characteristic under various conditions including photocurrent relaxation curves and photocurrent-illumination characteristics.

The voltage was applied to the sample 'S' from a potentiometer 'P'. A dry cell battery (3-9 volt) 'B' was connected to the potentiometer through the switch 'SW'. The output voltage from potentiometer was measured on a V.T.V.M. 'V', while the current readings were calculated from the IR drop across a precision resistor 'R' which was measured on a

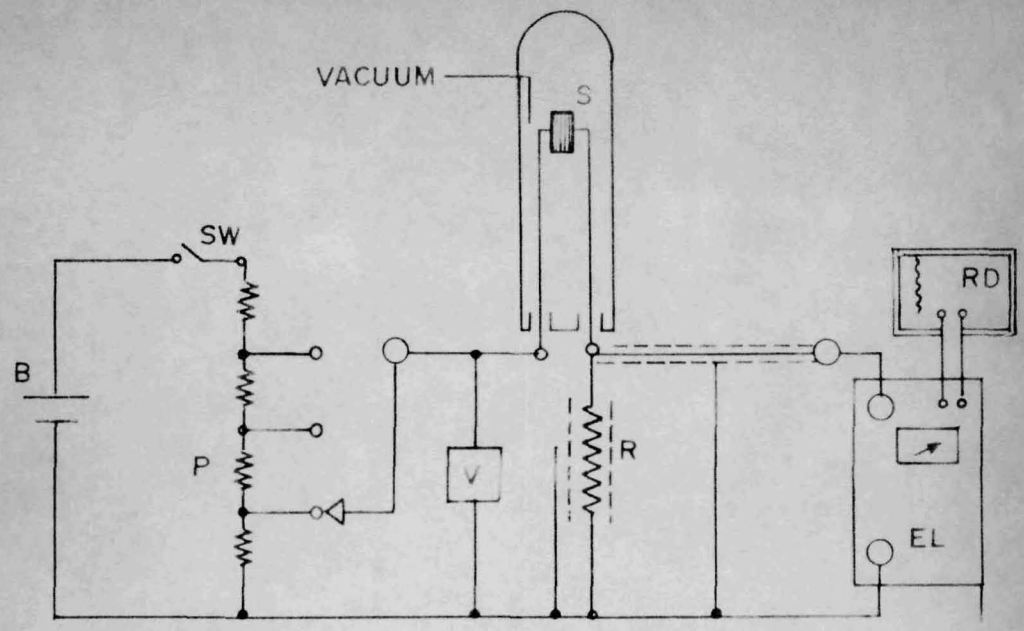


FIG. 2.5. CIRCUIT DIAGRAM FOR STEADY STATE I-V CHARACTERISTIC.

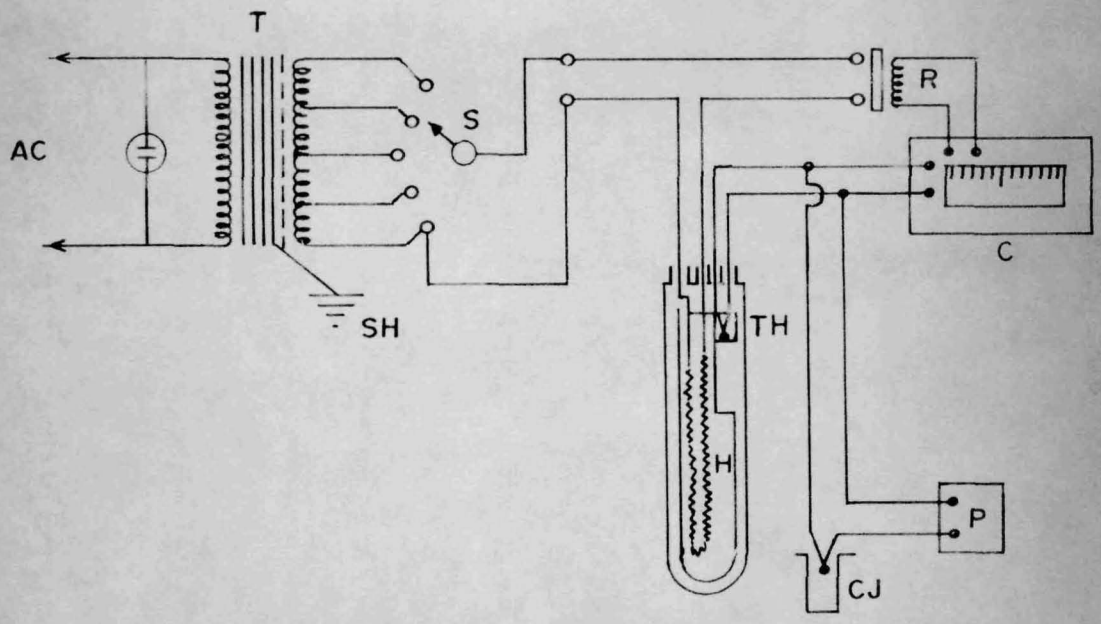


FIG. 2.6. CIRCUIT DIAGRAM FOR TEMPERATURE CONTROL

vibrating reed electrometer 'EL'. The electrometer also operated the recorder 'RD', which was used for recording current readings. The current-voltage characteristics were recorded by observing the current for various voltages applied across the sample. In making observations of voltage, care was taken to substract the small voltage observed across the electrometer and this voltage was always a small fraction of the applied voltage V.

The temperature dependence of current was measured by two methods :

(i) Under constant applied voltage in the temperature range from - 100° C upto 100° C.

The rate of heating of the sample was controlled by the use of a step down transformer with several tappings. The transformer was used in preference to a variac (variable auto-transformer) to provide a complete isolation of the sample circuit from the a.c. mains, which could cause spurious signals. The rate of temperature rise was sufficiently slow to enable readings to be taken at any constant temperature.

(ii) Under variable applied voltage and at various constant temperatures in the range from - 100° C upto 100° C.

It was possible to maintain constant temperature below 0° C because of the evacuated unit. Above 0° C the temperature was controlled by means of a chopper-bar temperature controller which could maintain the temperature constant within ± 5° C. The temperature was measured by means of a potentiometer.

In order to maintain low temperature the unit was first filled with dry argon and then liquid nitrogen was poured into the thermos flask. After getting the constant low temperature the unit was evacuated and measurements were taken.

Fig. 2.6 displays the circuit diagram for a temperature controller which operates as follows : The 220 volts a.c. is fed to the transformer 'T' which isolates the sample circuit and reduces the output voltage in steps (by means of the selector switch 'S') to give the desired control over the heating rate of the sample. The thermocouple 'TH' which is placed close to the sample is used for measuring the temperature with a PYE potentiometer 'P'. The temperature controller also uses the same thermocouple as temperature sensing element. By using this arrangement it was possible to maintain the temperature constant at any required value in the range of 0° to 200° C. In the figure, H denotes the heater (250 Ω), 'C' the chopper bar controller, 'R' the relay contact operated by the controller, 'CJ' the cold junction and 'SH' the earthed shield.

2.3.iv PHOTOCONDUCTIVE AND PHOTOVOLTAIC MEASUREMENTS

The photoconductivity of the samples of CdSe and CdTe was measured by using a d.c. voltage source and a steady illumination from a tungsten filament lamp. Various illumination intensities were applied by the use of a set of neutral density filters. The electrical circuit is the same as that used for the static I-V measurements described above.

The response of the samples was measured by an apparatus which consisted of a light source, focusing optics and a synchronous-motor driven chopper disc. Light interrupted by the rotating disc falls on the sample whose resistance changes with each pulse of light. The waveform is amplified and fed to an oscilloscope from which the response time (i.e. time taken to reach 0.63 of the maximum value) is easily calculated since the chopper frequency (20 cps) is known.

The open circuit photovoltage was measured by means of a vibrating reed electrometer with the input resistance of greater than 10^{12} ohms. The photocurrent under short circuit conditions could not be detected. This is attributed to the high internal resistance of the sample.

. . . . .

CHAPTER - 3

RESULTS AND DISCUSSION

Aluminium-cadmium selenide or telluride-gold sandwiches have been prepared on glass substrate by the vapour phase deposition technique described above. The pressure in the chamber was of the order of 10^{-5} - 10^{-6} Torr and the source temperature was approximately 750°C. The substrate was between 150 to 230° C. Deposited layers were annealed at 150-350° C under vacuum. The thickness of the semiconductor layer ranges from 0.5 to 1 micron.

These sandwiches show interesting bistable conductivity, switching and memory phenomena. Initially, the virgin samples (preformation stage) show a rectifier-like current-voltage characteristic. After an initial formation (post formation stage) they show bistable conductivity and cyclic switching between a high conductivity and a low conductivity state which takes place continuously under applied cyclic voltage. In what follows, we describe results of the detailed experimental investigation on both the pre- and post-formation stages of Al-CdSe (or CdTe)-Au sandwiches.

3.1 DYNAMIC I-V CHARACTERISTICS

3.1.i PRE-FORMATION

The dynamic I-V characteristics were measured on the set-up described earlier. The photograph of oscilloscope

record for CdSe in pre-formation stage is shown in Fig. 3.1 and that of CdTe in figures 3.2(a) and 3.2(b).

CdSe sandwich exhibits an asymmetric, rectifier-like I-V characteristics (curve I). All CdSe samples almost inveriably show the same behaviour. However, the I-V characteristics of Al-CdTe-Au sandwiches are rather sensitive to preparation conditions. We could distinguish two types of samples, one which shows non-linear but only slightly asymmetric I-V characteristic and has a large resistance of the order or 10^5 ohms in both directions (Fig. 3.2 a, curve I). For the other type there is a pronounced rectification observed (Fig. 3.2 b).

Al-CdSe-Au sandwiches are forward biased by making Au electrode negative, which is contrary to what one would expect on the basis of work function theory since CdSe is usually n-type material and Au has higher work function. In reverse bias, a rapid rise in current is observed beyond a certain voltage. The magnitude of this voltage varies to some extent from sample to sample. Some samples show an abrupt rise in current resembling a Zener diode (Fig. 3.3). However, large hysteresis effect follows this transition as can be seen from the figure.

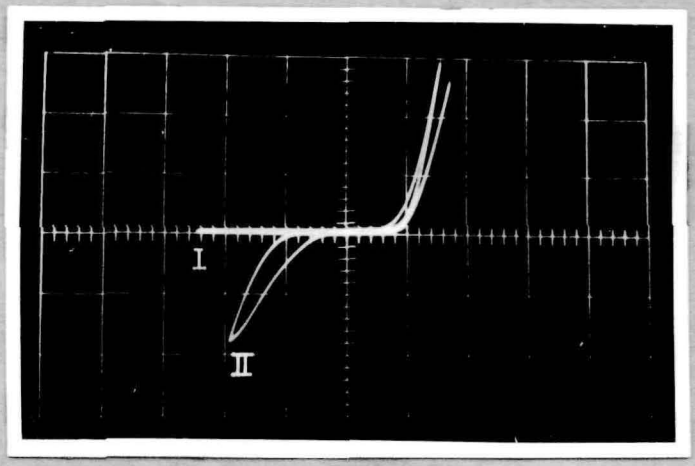


Fig. 3.1 Al-CdSe-Au sandwich (before formation) in dark (curve I) and under light (curve II). Horizontal : 10 v = 8 divs. Vertical : 1 mA = 1 div. Applied frequency 0.25 Hz.

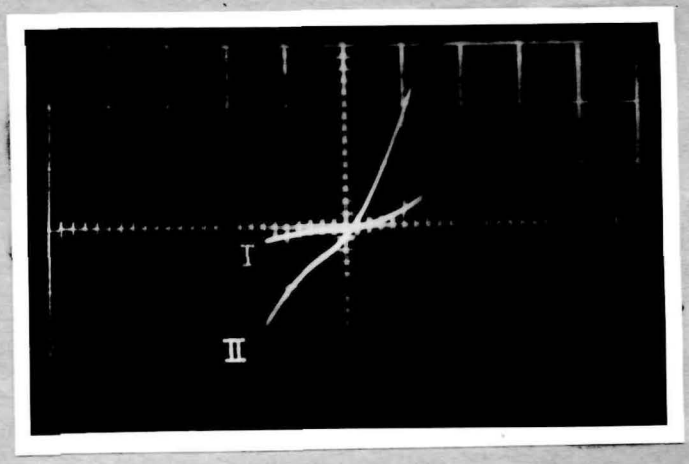


Fig. 3.2(a) Al-CdTe-Au sandwich, non-rectifying type, (before formation) in dark (curve I) and under light (curve II). Horizontal : 10v = 8 divs. Vertical : 0.14 mA = 1 div. Applied frequency 0.25 Hz.

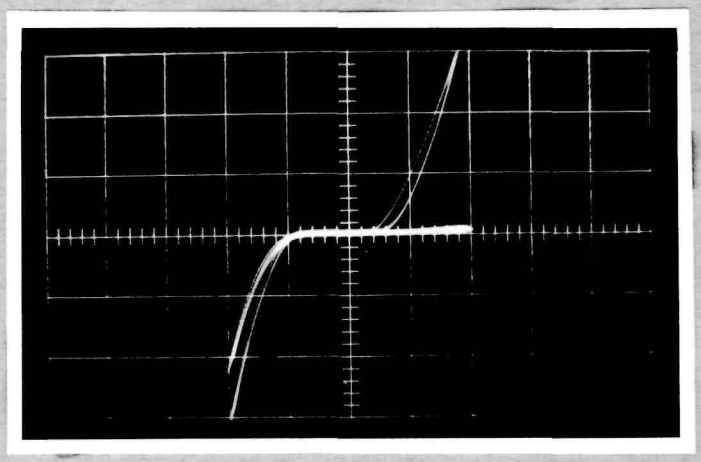


Fig. 3.2(b) Al-CdTe-Au sandwich rectifying type (before formation) in dark and under light. Horizontal : 10 v = 8 divs. Vertical : 0.11 mA = 1 div. Applied frequency 0.25 Hz.

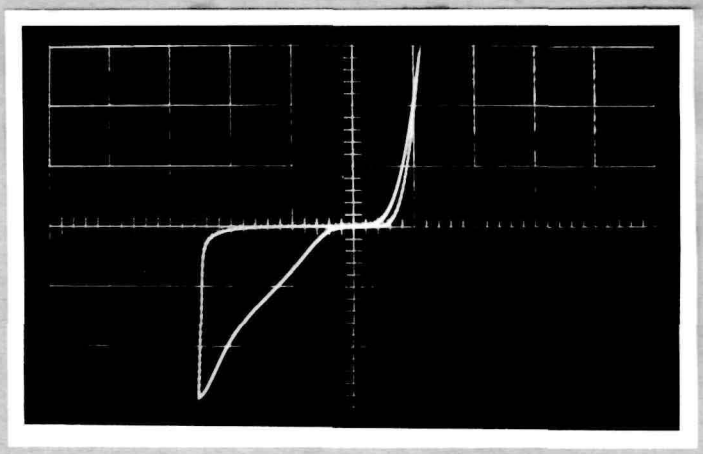


Fig. 3.3 Al-CdSe-Au sandwich (before formation) in dark, having large hysteresis effect. Horizontal : 10 v = 8 divs. Vertical : 5.2 mA = 1 div. Applied frequency 0.25 Hz.

The structure is highly photosensitive in the range of visible light, mainly when it is reverse-biased. Photocurrent increases rapidly with increasing applied reverse voltage (Fig. 3.1, curve II).

In Al-CdTe-Au systems, the sandwiches which show rectification (Fig. 3.2 b) have the properties very similar to the Al-CdSe-Au samples discussed above. However, contrary to CdSe, the telluride sandwich is forward biased when Au electrode is made positive. Like CdSe, this sample is also photosensitive mainly when reverse-biased (Fig. 3.2 b).

In Al-CdTe-Au system, the sandwiches, which do not show pronounced rectification (Fig. 3.2 a), show a pronounced photoconductivity and this is observed for both directions of applied voltage (Fig. 3.2 a, curve II).

3.1.ii. POST-FORMATION

If one applies a negative voltage on Al electrode (regardless whether it is base or counter electrode) of a value greater than a critical voltage (V_A), the sample switches from low conductivity state to a highly conducting ohmic state. It remains in this state as long as a certain critical voltage (V_c) of reverse polarity (i.e. Al+) is not exceeded. On exceeding this critical voltage

the sample switches back to the low conductivity state. Further increase in voltage (Al positive) does not cause any change and one has to make Al negative again and exceed the voltage V_A to switch back to the conducting state. On applying sufficient voltage of a small repetition frequency, the sample will switch from low to high conductivity state and vice versa in a cycle. The observed cycle would thus be OABOCDEDOAB ... for CdSe (Fig. 3.4) and OABOCDBOAB ... for CdTe (Fig. 3.5).

It is generally possible, to establish switching only if one can apply a sufficiently high negative voltage on the Al electrode without passing an excessive current. In other words, samples showing the behaviour of Fig. 3.2(b) and 3.3 for CdTe and CdSe respectively where current attains high values at fairly low negative voltage on Al electrode usually do not show formation to the switching state.

It is thus seen that in the post formation stage the sample can exist in either of the two stages : (i) EDOA (low conductivity state) or (ii) BOC (high conductivity state). The state (i) is attained after a positive voltage greater than V_c has been applied to the aluminium electrode and remains stable so long as the negative voltage V_A is not exceeded. It can be cycled any number of time

reversibly between the voltage V_A on the negative side and a corresponding voltage on the positive side. The state (ii) is attained after a negative voltage of magnitude greater than V_A has been applied and remains stable so long as the positive voltage V_C is not exceeded.

(a) Low conductivity state

Generally, the sample in the low conductivity state of the post-formation stage (i.e. state i described above) has higher conductivity than that in the pre-formation stage. Such a sample, whose conductivity has been enhanced on formation, loses the rectification characteristics partially and photosensitivity completely. However, there are some samples where the conductivity in the post-formation low conductivity state is nearly the same as that in the pre-formation stage. In such a case the original rectification and photosensitive characteristics are fully preserved. In such a sample the cyclic switching is destroyed under illumination (Fig. 3.6) and the I-V curve becomes OWONO. It may be concluded that in this case the formation process is not complete.

After repeated switching the sample may burn off giving rise to a high resistance, much higher than that in the pre-formation stage. Furthermore, in the case of

the switching established without change in I-V characteristic between pre-formation and post-formation stage, cited above, there has not been visible damage of the sandwich. In other case, i.e. when there is an appreciable formation, the sample usually shows some pin holes in the counter electrode. This is especially typical for samples which possess high resistance and have a higher thickness. However, if the initial switching takes place at low temperature (liquid nitrogen), the above-mentioned damage can be avoided.

(b) High conductivity state

When the voltage of the negatively biased Al electrode reaches V_A, the sample switches to the high conductivity ohmic state BOC (Fig. 3.4 and 3.5) accompanied by a large drop in the voltage. This is similar to what is observed in current controlled negative resistance (CCNR). The switching is a fast process estimated to take place in about 10^{-7} sec. for CdTe and 10^{-5} sec. for CdSe. In the high conductivity state, the sample has a resistance of 10-50 ohms. and is independent of voltage (ohmic state) and temperature.

The switching from C to D is associated with a large drop of current as is usually observed in the voltage controlled negative resistance (VCNR).

This switching phenomenon is best performed at frequencies upto 2.5 c/sec. On applying higher frequencies upto 250 c/sec. the same behaviour is more or less obtained although at times switching may be missed out. At still higher frequencies switching disappears completely and the sample cycles on the path AOE. Consequently if one increases voltage of such a high frequency ($>$ 250 Hz) in order to produce switching sample usually gets damage. However, if the sample is kept at liquid nitrogen temperature one can produce cyclic switching even at frequencies upto 2500 c/sec.

At this stage it may be worthwhile mentioning that the first I-V trace of a freshly prepared virgin sample is sometimes ohmic with slope similar to BOC of Figs. 3.4 and 3.5. This, however, immediately switches to the pre-formation characteristics discussed earlier. This transformation takes place when Al electrode is made positive as in the case of the post-formation stage just discussed.

It may also be relevent to mention that Au-CdSe (or CdTe)/-Au sandwiches prepared in a similar way always show the ohmic high conductivity I-V curve. However, it has never been possible to convert them to the high resistive state from which cyclic switching could be

established. From this, it is concluded that Au-CdSe or Au-CdTe contacts prepared under our experimental conditions are always ohmic. This has an important bearing on the properties of our sandwiches and would be discussed in detail later.

In what follows we discuss these results in detail in the following sequence :

Steady state I-V characteristics, temperature and voltage dependence of conduction and switching.

Relaxation effects.

Photovoltaic and photoconducting properties.

Pulsed measurements.

Mechanism.

3.2 STEADY STATE I-V CHARACTERISTIC

In order to examine the mechanism of conduction in the samples, D.C. measurements were taken under various conditions allowing sufficient time for establishment of equilibrium. The experimental set up used for this measurement is described earlier.

3.2.1 PRE-FORMATION STAGE

Figures 3.7 and 3.8 show the plots of steady state I-V characteristic of Al-CdSe-Au and Al-CdTe-Au samples respectively at room temperature in dark (CdSe) and under light too (CdTe) on a linear scale. It can be seen that there is not much difference between these and the corresponding dynamic characteristics.

Figure 3.9 gives the I-V plot (on a linear scale) for a Al-CdTe-Au sandwich at various temperatures. It can be seen that the sample shows a strong voltage and temperature dependence. It is generally found that higher the resistance the greater is the temperature dependance. Thus for an Al-CdSe-Au sandwich, there is only a slight temperature dependance in the forward direction but an appreciable dependance in the reverse direction. The same is true for Al-CdTe-Au sandwiches

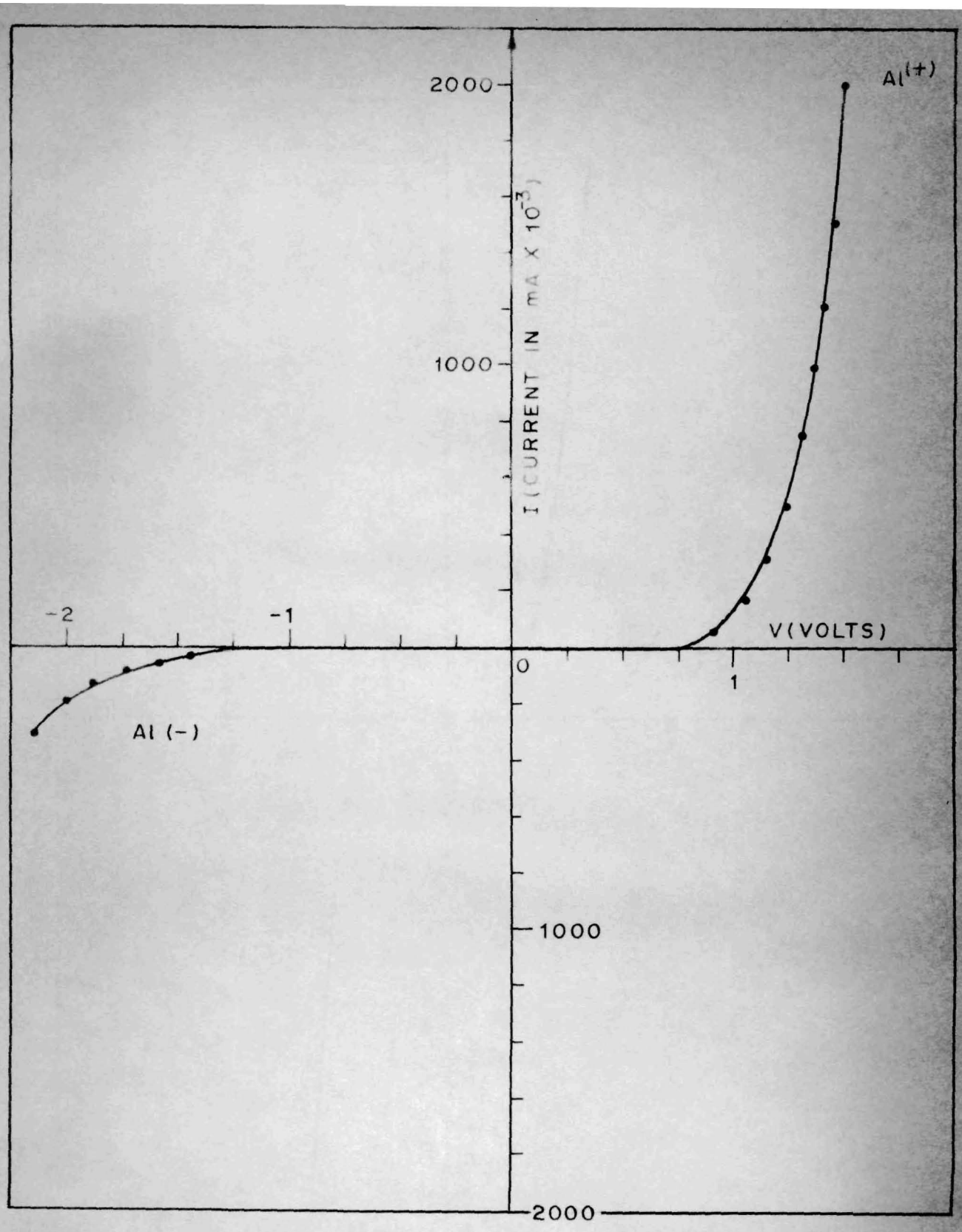


FIG. 3.7. STEADY STATE I-V CHARACTERISTIC OF Al-CdSe-Au IN DARK.

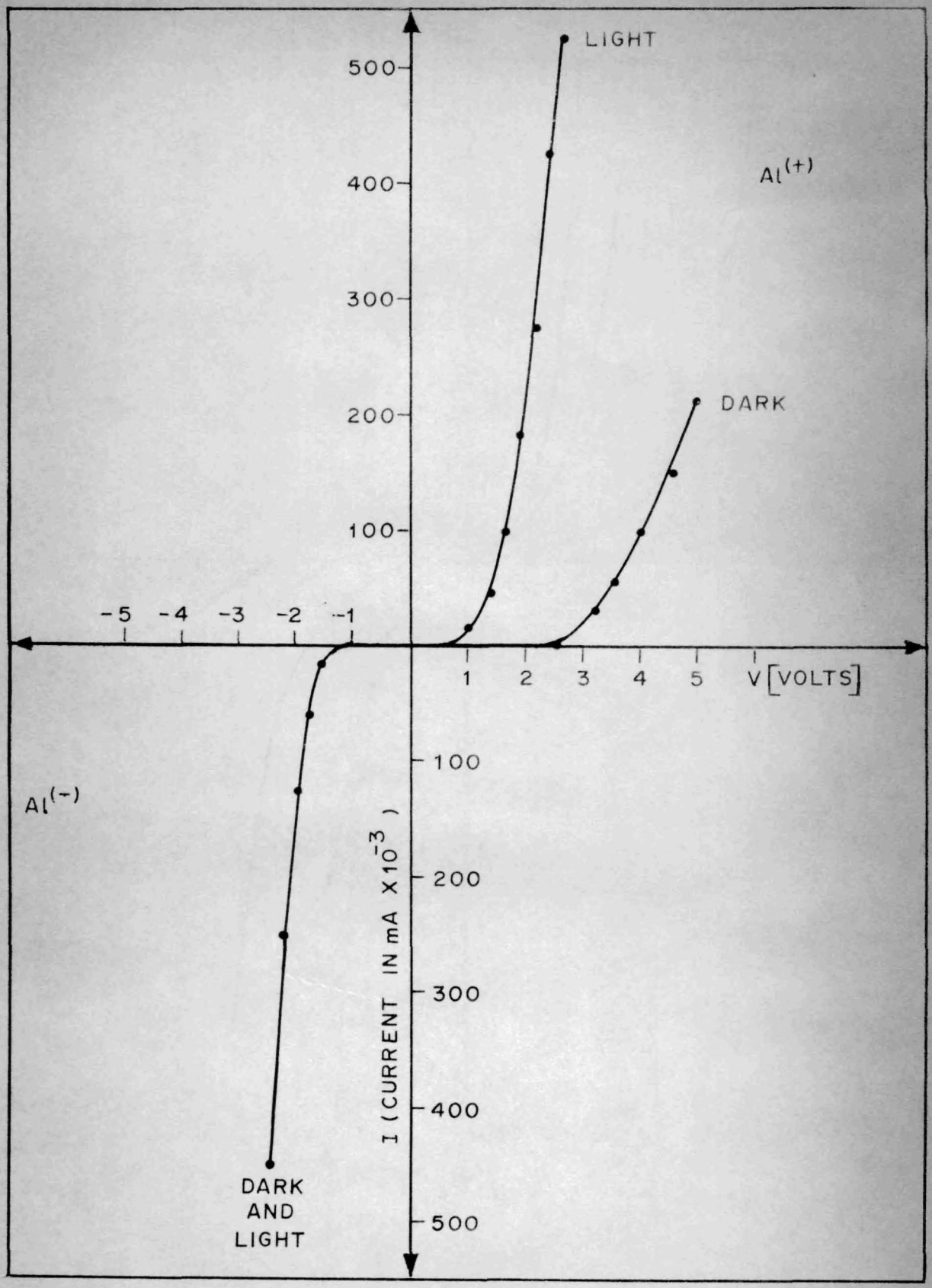


FIG. 3.8. STEADY STATE I-V CHARACTERISTIC OF Al-CdTe-Au IN DARK AND UNDER LIGHT.

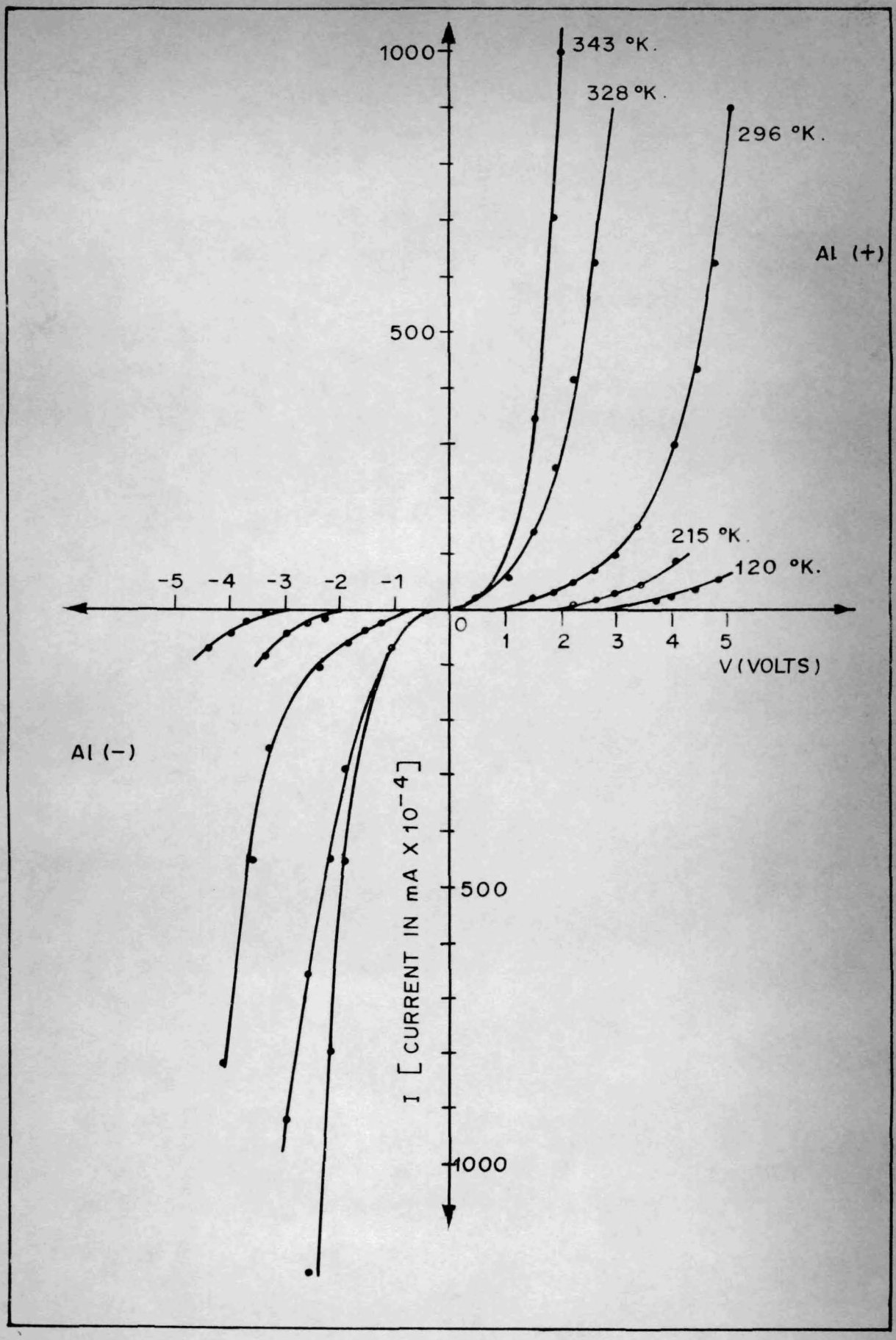


FIG. 3.9. STEADY STATE I-V CHARACTERISTIC OF Al–CdTe–Au IN DARK AT VARIOUS TEMPERATURES.

which show rectification. On the other hand Al-CdTe-Au sandwiches which show high resistance on both sides show a strong temperature dependance in both directions (Fig. 3.9).

We now attempt to analyse these results in the following sequence :

(i) Direction of rectification in the light of work-function theory and other properties of CdSe and CdTe.

(ii) Temperature and voltage dependance of current and the light they throw on the mechanism of conduction.

(a) Direction of rectification

For Al-CdSe-Au system, the CdSe-Au contact has been found to be ohmic under our experimental conditions. This would mean that the rectifying barrier responsible for the observed asymmetric I-V characteristic is present at the Al-CdSe interface. In that case the direction of rectification can be explained if it is assumed that our CdSe is n-type which indeed appears to be well-supported by the published results (see page 62). However, our finding that the Al-CdSe contact is blocking whereas the Au-CdSe contact is ohmic conflicts with some earlier observations. For example Learn et al[109] have found

that Al-nCdS contact is ohmic. On this basis, it is likely that Al would give ohmic contact to CdSe which is also n-type with a comparable work function. In fact Terasaki et al[110] report experimental confirmation to this effect. However, they also report that in some cases Al does not give ohmic contact to CdS. Adirovich et al[111] have also observed that Al gives a blocking contact to vacuum deposited CdS films.

There are various ways in which an expected ohmic contact may become rectifying. The existance of surface states could be responsible for the observed rectification irrespective of the nature of the metal semiconductor contact. In addition, a barrier can also be created due to a foreign material on the surface.

On the other hand, the Au-CdSe contact which is expected to be blocking on the basis of work function theory has become ohmic. Au has a high work function and its Fermi level is expected to lie lower than that of n-CdSe. On making the Au-CdSe contact, a blocking barrier is therefore expected to arise at this contact. In fact, for many years Au has been used as blocking electrode to CdS and CdSe[112]. However, specially in the case of thin evaporated films, gold may fail to give blocking contacts.

Zuleeg and Muller[113] have observed that Au, if it is deposited as the base electrode, does not give blocking contact to CdS. They believe that there is a tendency for an initial adhesion by Cd atoms to the Au contact. This Cd layer results in n^+ region and thereby forms an ohmic contact.

Nakai et al[114] have found that Au electrode deposited on CdSe films gives ohmic contact. The authors attribute this to the reduction of the work function of the upper surface of CdSe by gas adsorption. Ohmic Au-CdS contact has been observed by Bujati[115] too.

In our case, Au-CdSe contact is ohmic apparently due to the formation of a highly degenerate semiconductor at the surface, due to the diffusion of impurities. High donor concentration near the surface makes the barrier extremely narrow and hence transparent to carriers.

In regard to Al-CdTe-Au sandwiches we have already mentioned about two extreme cases viz. (i) which exhibits well pronounced rectifier-like characteristic, and (ii) which is highly resistive in both directions and shows only slight asymmetry in its I-V curve. Some sandwiches may show intermediate characteristics also.

The first class appears to be analogous to the case of Al-CdSe-Au discussed above and appears to have the barrier at the Al-CdTe interface. As has been mentioned above, the Au-CdTe-Au sandwich prepared by us under the present experimental conditions shows ohmic behaviour. By changing one gold electrode to aluminium (Al-CdTe-Au sandwich) rectification appears. It is, therefore, reasonable to conclude, once again, that, the barrier is at Al-CdTe interface. The observed direction of rectification can then be explained if CdTe is p-type. This is not unreasonable because it is well-known that CdTe can be either n-type or p-type (see page 62).

The second class of Al-CdTe-Au sandwiches may owe their property of high resistance in both directions either to the existence of a high series resistance (i.e. due to an insulating layer or due to a high resistance of the bulk CdTe) or to the existence of two opposing barriers. We would revert back to this problem later while discussing other results.

(b) Mechanism of conduction

In the Chapter on "Introduction" we have already discussed the various possible mechanisms of conduction in thin film of insulators and semiconductors. A comparison

of various equations reveals that a study of current as a function of voltage and temperature can give an insight into the mechanism of conduction. The characteristic features of our samples is a high temperature and voltage dependence of conduction. This, therefore, led us to look for mechanisms which involve strong temperature as well as voltage dependence. Such a dependence of the reverse diode current can be obtained if the effect of Schottky image force or tunnel penetration is invoked, because the diode current in reverse direction in the absence of these, shows a saturation and becomes independent of voltage.

Schottky[116] has deduced an expression for the emission current density from a metal into vacuum when the metal is heated as well as subjected to a negative potential. The negative potential lowers the barrier height due to the image force and temperature raises the energy of the electrons to enable them to cross the barrier. The current density J in such a case is given by :

$$J = AT^2 \exp\left(-\frac{\phi}{kT}\right) \exp\left[\frac{q}{2kT}\left(\frac{qE}{\pi K}\right)^{1/2}\right]$$

where : A = Richardson constant.
T = Temperature in ^{o}K.
ϕ = Barrier height.
k = Boltzmann constant.
q = Electronic charge.
E = Applied field.
K = Dielectric constant.

Emtage and Tantraporn[117] have reported an analogous mechanism for the electron emission in insulators or semiconductors when there is a barrier present at the contact. The electrons from metal cross over the barrier with the help of thermal energy, the barrier itself being lowered by the field at the contact. However, the field at the contact is governed by the nature of barrier region and its width.

The effect of Schottky emission on current in a reverse biased metal-semiconductor diode has already been discussed in Chapter I and the expression has the form :

$$J = A'T^2 \exp(-\phi/kT) \exp\left[\frac{\alpha(V_D + V_B)^{1/4}}{kT}\right]$$

(see page 15) where A' is the Richardson's constant for emission from metal to semiconductor which may be different from A, the Richardson constant for metal-vacuum emission (A = 120 Amp/cm^2 - degree^2), ϕ the barrier height, α a constant, V_D diffusion voltage and V_B voltage drop across the barrier.

In practice, the applied voltage V_B is appreciably higher than V_D. Furthermore, assuming that V_B V, the applied voltage, we have

$$J \simeq A'T^2 \exp(-\phi/kT) \exp(\alpha V^{1/4}/kT)$$

$$\text{or } \log J/T^2 = \log A' - \phi/kT + \alpha V^{1/4}/kT$$

If $\log J/T^2$ is plotted against $1/T$ at a fixed voltage, the plot should be a straight line with intercept equal to $\log A'$ and the slope equal to $1/k\,(\alpha V^{1/4} - \phi)$. Furthermore, if $\log J$ is plotted against $V^{1/4}$ at a fixed temperature then also the plot should be a straight line with the intercept $(\log A'T^2) - \phi/kT$ and the slope α/kT. From the two intercepts it is therefore possible to obtain the values of the emission constant A' and the barrier height.

If, on the other hand, tunnel penetration controls the modulation of the barrier height, one can show, on the basis of arguments similar to above, that $\log J$ vs $V^{1/2}$ should be a straight line[4].

Figure 3.10 shows the plot $\log J/T^2$ as a function of $1/T$ for two Al-CdTe-Au sandwiches in the pre-formation stage with Al positive and gold negative. These samples belong to the non-rectifying class and have high resistance in both directions. A linear relationship is observed down to 280° K. The intercept for the two graphs (A) and (B) give $\log A'$ as 1.3 and 3.1 respectively. The

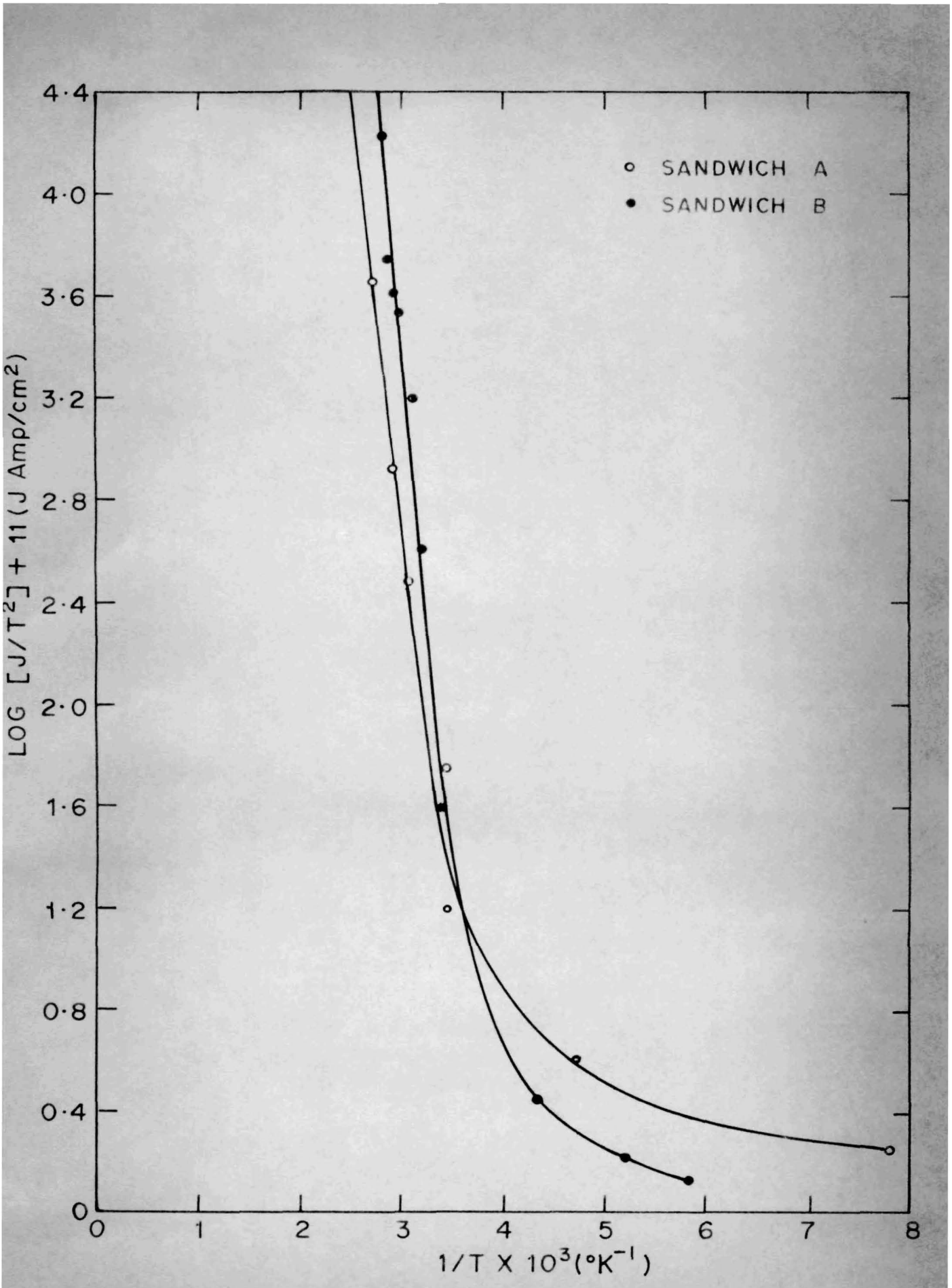


FIG. 3.10. LOG J/T^2 VS. $1/T$ CHARACTERISTIC OF TWO Al-CdTe-Au SANDWICHES [Al POSITIVE].

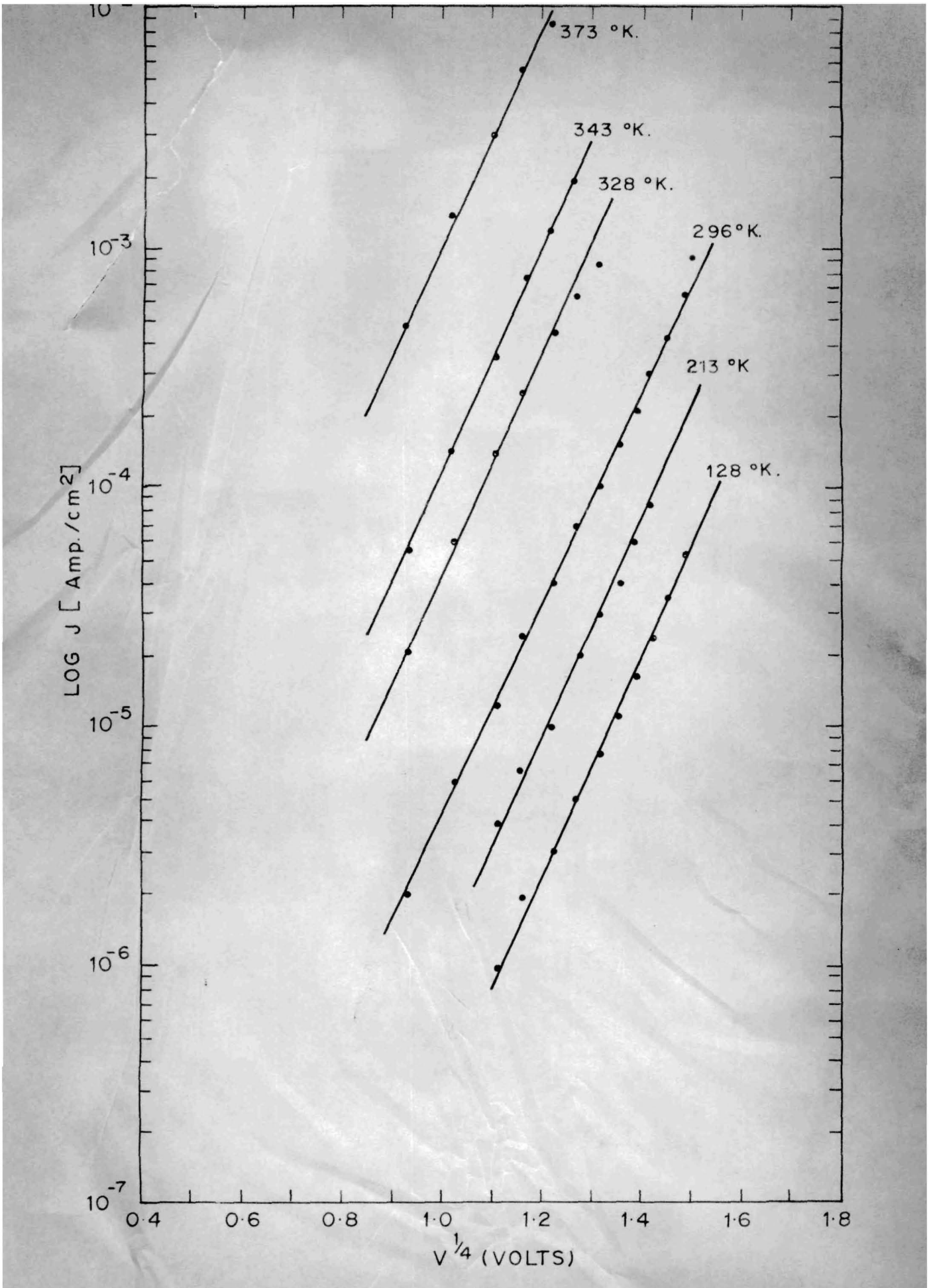


FIG. 3. 11. LOG J VS. $V^{1/4}$ CHARACTERISTIC OF Al-CdTe-Au SANDWICH [Al POSITIVE].

different I-V curves of Fig. 3.9 and curve A of Fig. 3.10 and that of 3.11, 3.12 and 3.13 have been obtained from the same sample.

Figure 3.11 shows the plot of log J as a function of $V^{1/4}$ for sample A at various temperatures. It can be seen that the experimental points are quite close to the best straight line in each case. Using the incercept from the graphs and the value of log A' obtained above, the values of ϕ have been calculated for 373°, 343°, 328° and 296° K and are given below :

Temp. (°K)	ϕ (eV)	Mean ϕ (eV)
373	1.03	
343	1.01	.99 ± .04
328	0.99	
296	0.95	

TABLE I

Dark current as a function of temperature for the sandwich A at 2 volts

$T^{o}K$	$1/T \times 10^{3}\ K^{-1}$	J Amp/cm^2		$\log (J/T^2) + 11$	
		Al(+)	Al(-)	Al(+)	Al(-)
128	7.81	3.0×10^{-7}	5.0×10^{-7}	0.26	0.48
213	4.70	1.9×10^{-6}	6.0×10^{-6}	0.62	1.12
288	3.47	1.3×10^{-5}	-	1.20	-
296	3.38	3.5×10^{-5}	5.6×10^{-5}	1.60	1.81
328	3.05	3.3×10^{-4}	3.2×10^{-4}	2.49	2.48
343	2.92	1.0×10^{-3}	5.8×10^{-4}	2.93	2.69
373	2.70	6.4×10^{-3}	3.0×10^{-3}	3.66	3.33

Sample has 0.5μ electrode spacing and 0.1 cm^2 area.

TABLE II

Dark current as a function of temperature for the sandwich B at 2.5 volts

$T^{o}K$	$1/T \times 10^{3}\ K^{-1}$	J Amp/cm^2		log (J/T^2) + 11	
		Al(+)	Al(-)	Al(+)	Al(-)
193	5.18	5.0×10^{-7}	1.0×10^{-6}	0.13	0.43
217	4.60	-	2.5×10^{-6}	-	0.72
231	4.33	1.5×10^{-6}	8.0×10^{-6}	0.45	1.18
246	4.07	-	1.3×10^{-5}	-	1.33
260	3.76	-	3.4×10^{-5}	-	1.70
281	3.56	-	8.0×10^{-5}	-	2.01
293	3.41	4.8×10^{-5}	1.6×10^{-4}	1.75	2.27
310.5	3.22	3.9×10^{-4}	4.1×10^{-4}	2.61	2.63
321.5	3.11	1.6×10^{-3}	8.8×10^{-4}	3.20	2.93
333	3.00	3.8×10^{-3}	1.4×10^{-3}	3.54	3.10
345	2.90	5.0×10^{-3}	2.2×10^{-3}	3.62	3.27
355.5	2.81	7.0×10^{-3}	1.0×10^{-2}	3.74	3.90
367	2.79	1.3×10^{-2}	2.3×10^{-2}	3.98	4.23

Figure 3.12 shows a plot of log J as a function of $V^{1/2}$. Here also we get a reasonably good straight line in the range of higher voltages and, in fact, it seems very difficult to decide whether log J is proportional to $V^{1/2}$ or to $V^{1/4}$. A correct dependence would be $\log J \simeq V^n$ where 'n' lies in the range of 0.50 to 0.25. In other words, one cannot exclude any of the two mechanisms viz. the image force and tunnel effect. Actually, it may be too unrealistic to expect that any one mechanism controls the lowering of the barrier height in a heterogeneous sample such as ours which may show considerable lateral variations. As is well-known, the tunnel effect depends very sensitively on the barrier thickness and if the sample shows a variation in the thickness of the barrier along the contact area, then there will be a considerable variation in the current density from region to region and in some regions of large barrier thickness the effect of image force might predominate whereas in other regions of small barrier thickness tunnel effect might control the barrier height modulation. The situation is further complicated by the fact that there may be small barrier-free contacts where Ohm's law might be obeyed. Even the theoretical equations which we have used for interpreting our results have been deduced under strong simplifying assumptions. One such assumption is

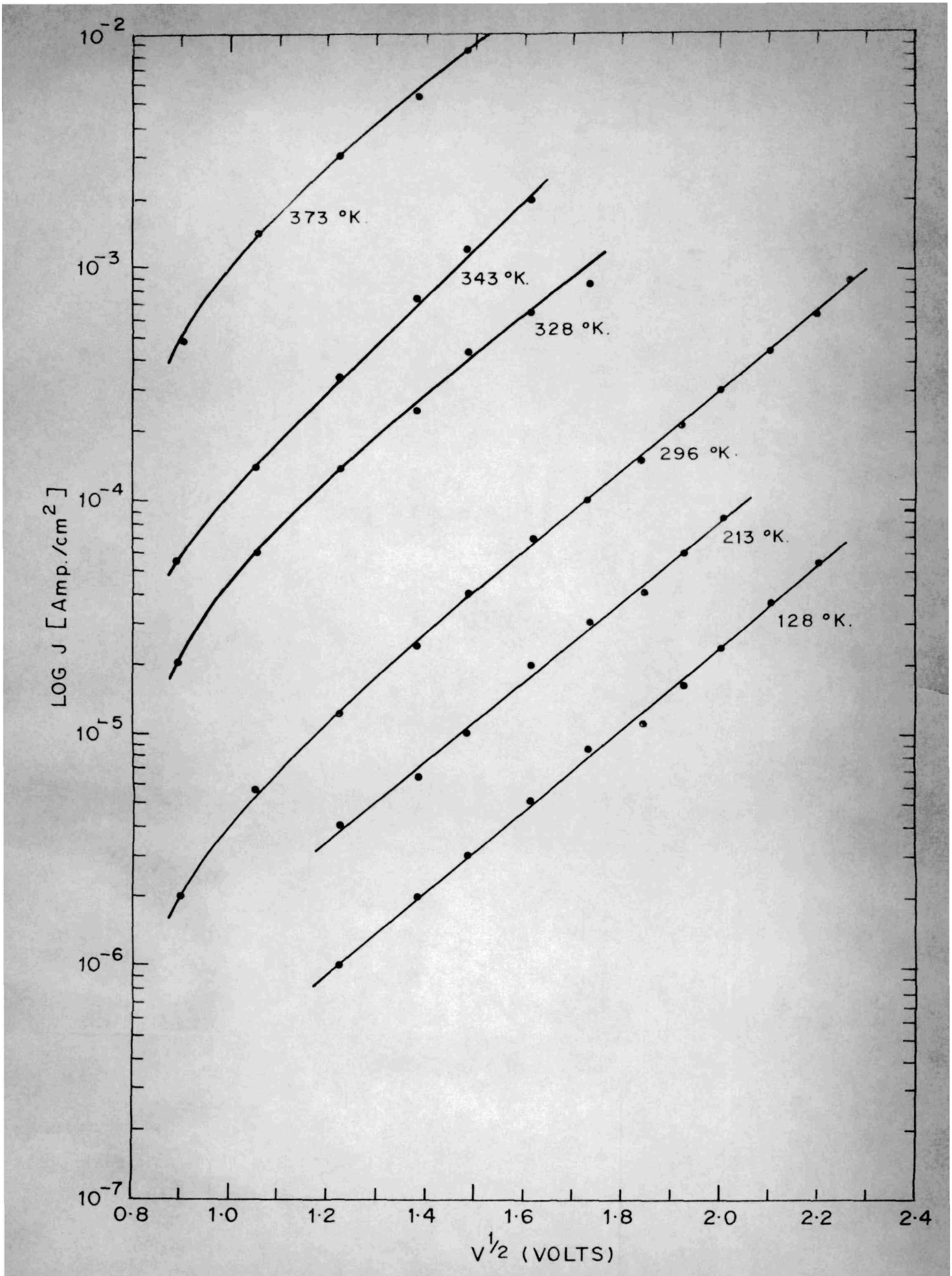


FIG. 3.12. LOG J VS. $V^{1/2}$ CHARACTERISTIC OF Al-CdTe-Au SANDWICH [Al POSITIVE].

that the electron occupation of the surface states is itself not a function of current flowing. This might not be true in actual practice.

However, the linear relationship between $\log J/T^2$ and $1/T$, and a fairly reasonable value of $\log A'$ seem to us strong enough evidences to justify the conclusion that a barrier is present and the conduction is due to the carriers crossing the barrier. Furthermore, this barrier is subject to corrections due to image force and tunnel penetration at higher voltages so that the I-V relationship does not show a saturation but a strong voltage dependence.

The plot of $\log J/T^2$ vs $1/T$ for the above two samples with Al negative and gold positive is shown in Figure 3.13. Here, also one observes a strong temperature dependence and at higher temperatures the plot is linear. However, the departure from linearity sets in at a slightly higher temperature than in the previous graph i.e. Figure 3.10 (330° K as compared to 280° K). The intercept and the slope of the high temperature part of the graph have approximately the same value as in the previous case.

The departure from linearity in the $\log J/T^2$ vs $1/T$ plots at low temperatures for either direction of applied

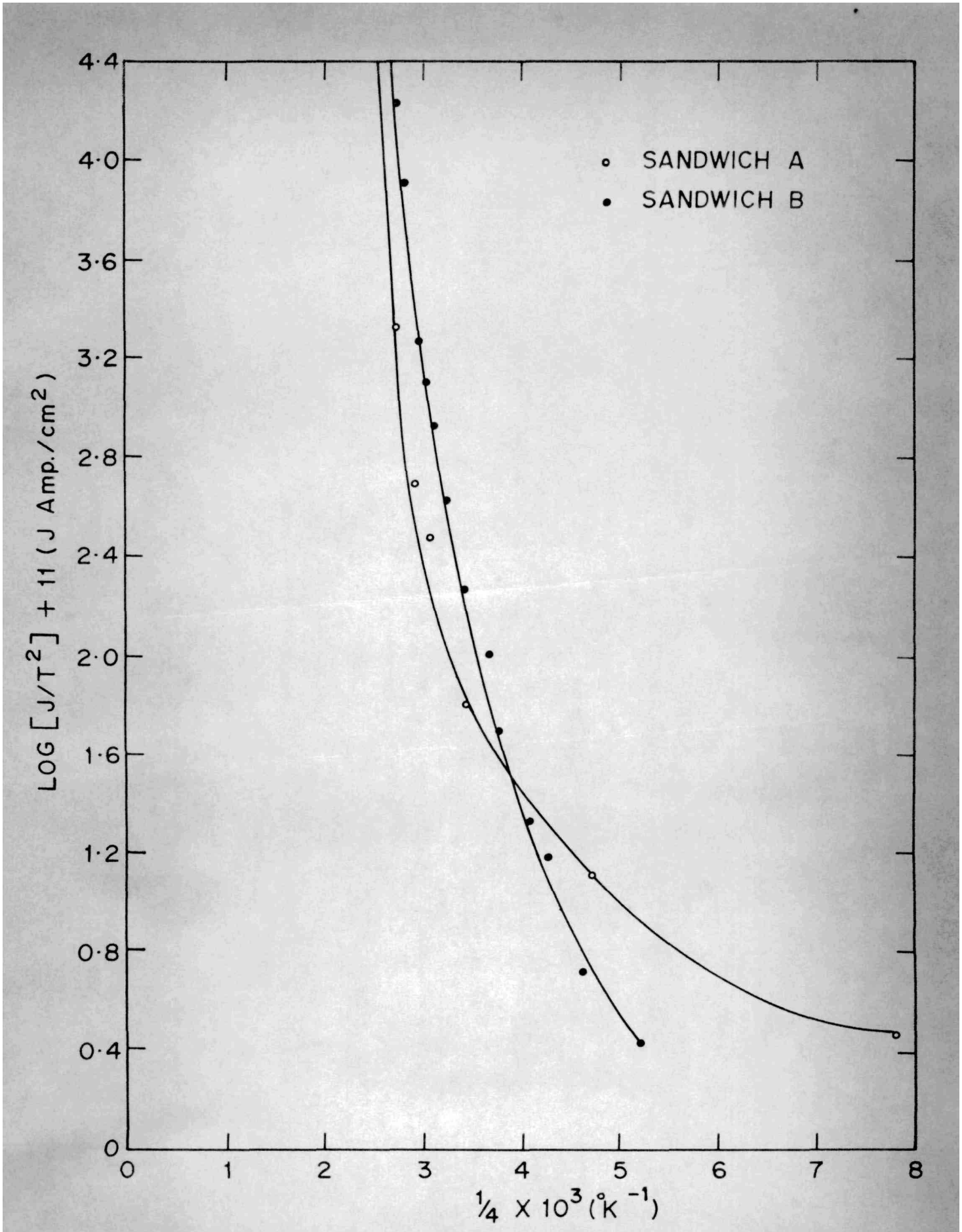


FIG. 3.13. LOG J/T^2 VS 1/T CHARACTERISTIC OF TWO Al-CdTe-Au SANDWICHES [Al NEGATIVE].

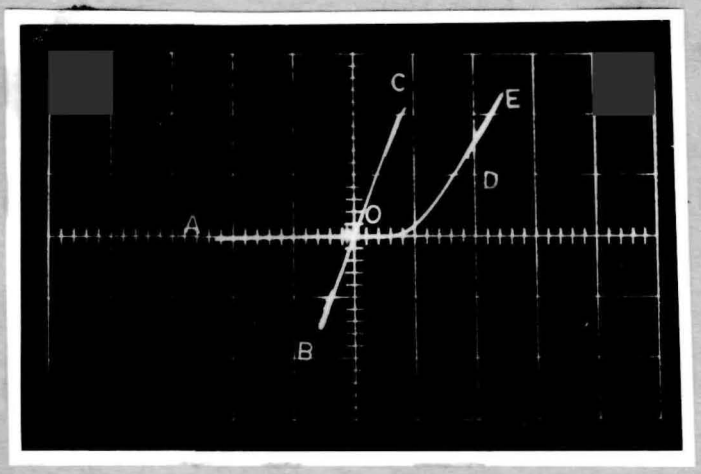


Fig. 3.4 Al-CdSe-Au sandwich showing the switching phenomenon (after formation) OABOCDEDOAB ... in dark. Horizontal : 10 v = 5 divs. Vertical : 11 mA = 1 div. Applied frequency 0.25 Hz.

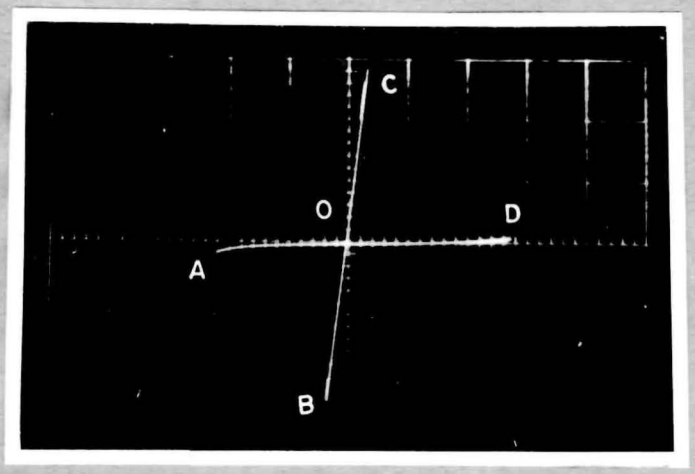


Fig. 3.5 Al-CdTe-Au sandwich showing the switching phenomenon (after formation) OABOCDOAB ... in dark. Horizontal : 10 v = 8 divs. Vertical : 4.8 mA = 1 div. Applied frequency 0.25 Hz.

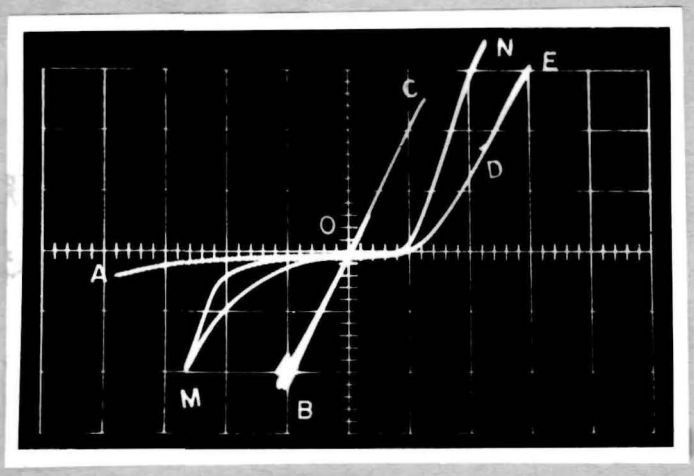


Fig. 3.6 Al-CdSe-Au sandwich showing the switching (after formation) OABOCDEDO ... in dark, and its disappearance under light OMONO. Horizontal : 10 v = 8 divs. Vertical : 7.3 mA = 1 div. Applied frequency 0.25 Hz.

voltage can be attributed to small islands of conducting, barrier-free regions. Along the contact area, there appears to be regions where the barrier is so small that one gets ohmic conduction or is so thin that conduction is possible due to tunneling. These might arise due to inhomogeneous distribution of impurities. No doubt, the fractional area covered by such regions would be relatively small. Thus at high temperatures when there is a considerable conductivity across the barrier, the relative contribution from the barrier-free region would be small and would, therefore, be not able to change the overall current temperature relationship. At low temperatures, however, when the conductivity across the barrier is considerably decreased, the relative contribution from the barrier-free region starts predominating. This conductivity being nearly temperature independent, the total current remains constant with temperature. A similar behaviour has been observed by Pollack[118] in thin Al_2O_3 films. He has explained this result as due to predominance of tunneling at low temperature when Schottky field emission becomes too small.

We now take up the voltage and temperature dependence of sandwiches which show pronounced rectification. All Al-CdSe-Au and class 1 (i.e. Figure 3.2 b) of the

Al-CdTe-Au sandwiches belong to this group. Under reverse bias, i.e. when Al electrode is negative in case of CdSe and positive in case of CdTe sandwiches, the characteristics are very much similar to what has already been discussed above. The plot of log J vs $V^{1/4}$ is a straight line (Figure 3.14). The value of ϕ as calculated from the intercept using the value of emission constant as 120 amp/cm^2-degree^2 turns out to be 1.0 ev. for sample A and 1.1 ev for sample B (both CdSe sandwiches). These values are close to that got for Al-CdTe-Au sandwiches.

For the forward direction, however, there is a marked difference. As already mentioned, in this case, the current is nearly independent of temperature. The forward current density is given by (see page 14)

$$|J| \simeq AT^2 \exp\left(-\frac{\phi - e|V_B|}{kT}\right)$$

Thus at forward voltages when $V_B \simeq \phi/e$, the argument of the exponential term vanishes and J becomes nearly independent of temperature.

Figure 3.15 shows the plot of log J as a function of V for the forward direction. As expected, the plot is linear at high voltages. However, the slope is much less

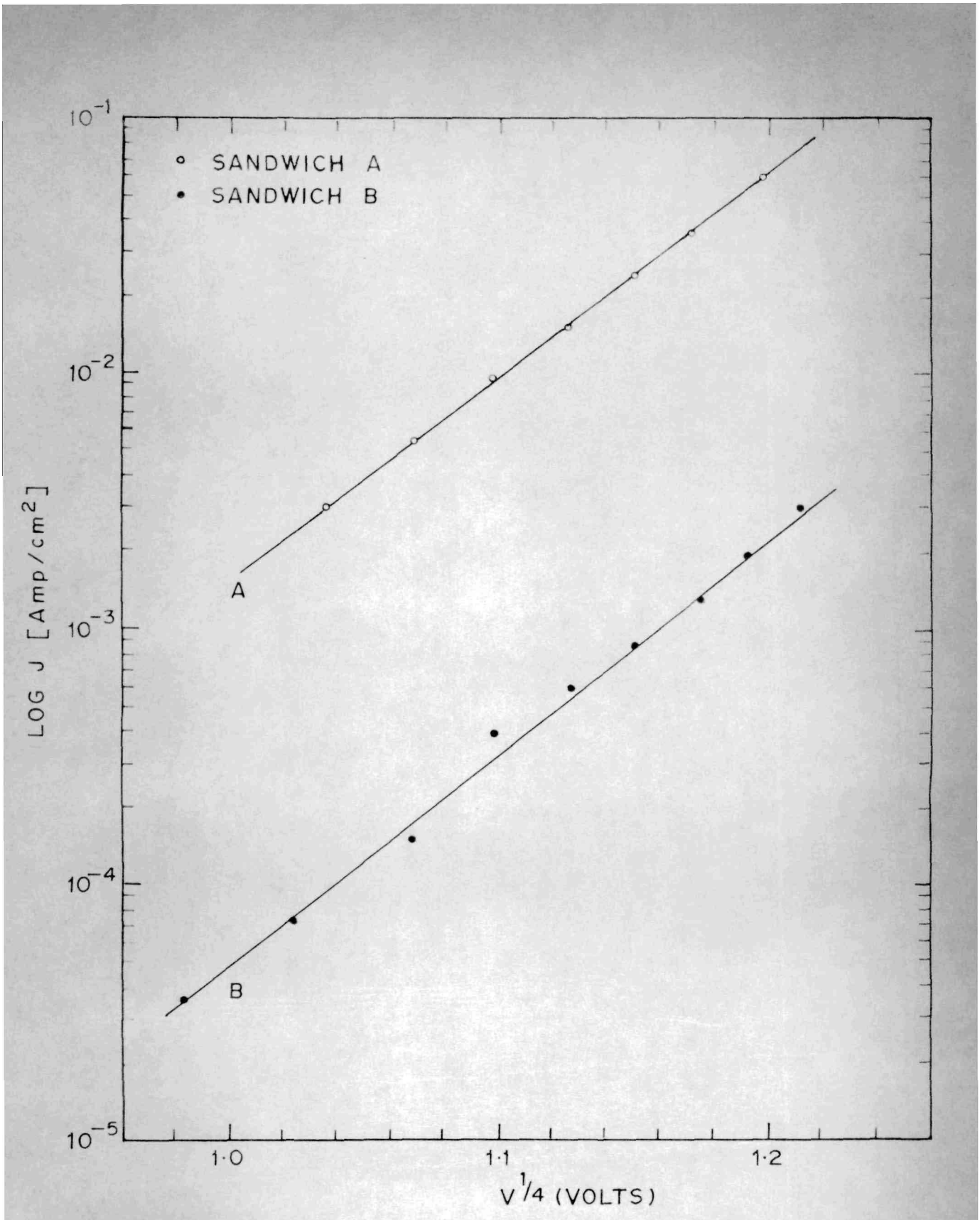


FIG. 3. 14. LOG. J VS. $V^{1/4}$ CHARACTERISTIC OF TWO Al-CdSe-Au SANDWICHES FOR REVERSE DIRECTION [Al NEGATIVE].

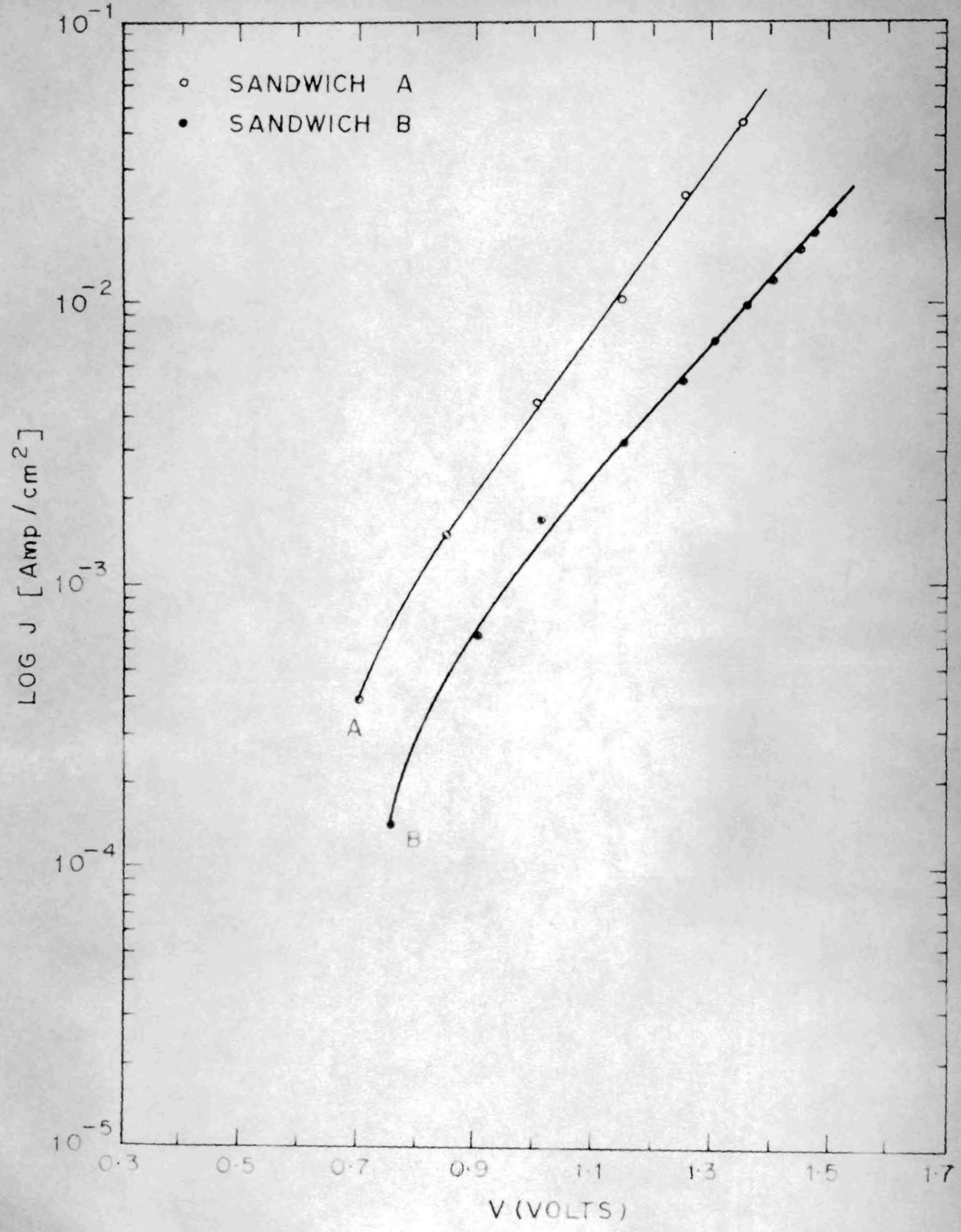


FIG. 3.15. LOG. J VS. V CHARACTERISTIC OF TWO Al-CdSe-Au SANDWICHES FOR FORWARD DIRECTION [Al POSITIVE]

than the expected value of e/kT. Such departures from the ideal value is quite common and can be attributed to non-uniform barrier height, spreading resistance and such other departures from ideal conditions. Johnson, et al[119] have treated the problem theoretically assuming an exponential distribution function of areas of different barrier heights. They have shown that any value of slope between zero and e/kT can be expected depending on the value of parameters controlling the distribution function. Numata[120] has attributed the departure of slope from ideal value to the base contact which becomes increasingly important at higher forward voltage.

3.2.ii. TIME DEPENDENCE OF CURRENT

It has been found that in the virgin state, current changes with time for any particular applied voltage. Both Al-CdTe-Au and Al-CdSe-Au sandwiches exhibit this time effect. After switching is established samples which have been 'formed' do not show any time dependence either in the low conductivity or in the high conductivity states. On the other hand, if the switching has been established without 'formation' then the time dependence remains just as in the 'virgin' samples.

Time effect in 'unformed' samples is fairly complex and its behaviour varies from sample to sample

but, in general this effect is characterised by a slow rise of current in reverse-biased diode and fast rise followed by a slow decay in the forward direction. CdTe sandwiches which show rectification (class i, page 94) usually do not exhibit the decay of current in forward bias. However in extremely rectifying cases there could be a slight decay in current with time. Rise of current with time is observed in the rectifying type CdTe and Cd Se diodes when they are reverse biased and in non rectifying type CdTe for both directions. Slow decay is found mainly in CdSe under forward bias.

The slow rise of current with time appears to be exponential. The time required to reach the saturation value is not constant but varies from sample to sample. The general behaviour is given in Fig. 3.16 and Fig. 3.17, for CdSe and CdTe respectively.

Decay of current, as already stated above, has been found in CdSe forward-biased samples. In this case, the current attains the saturation value faster than in the case of current rise. The saturation current is approximately one-third of the maximum initial current (see Fig. 3.18).

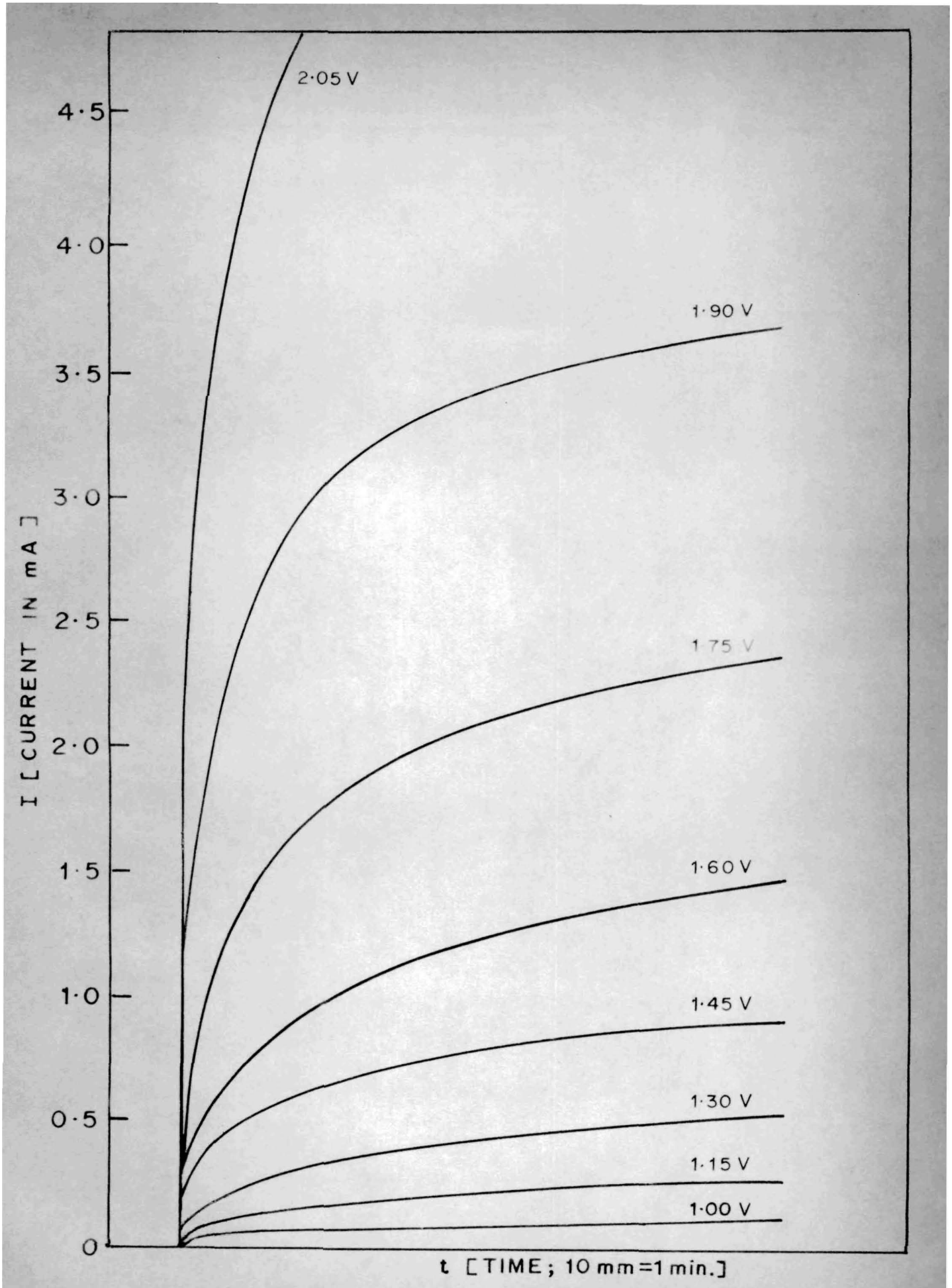


FIG. 3. 16. RISE OF CURRENT WITH TIME IN CASE OF A REVERSE BIASED Al-CdSe-Au SANDWICH (Al-NEGATIVE).

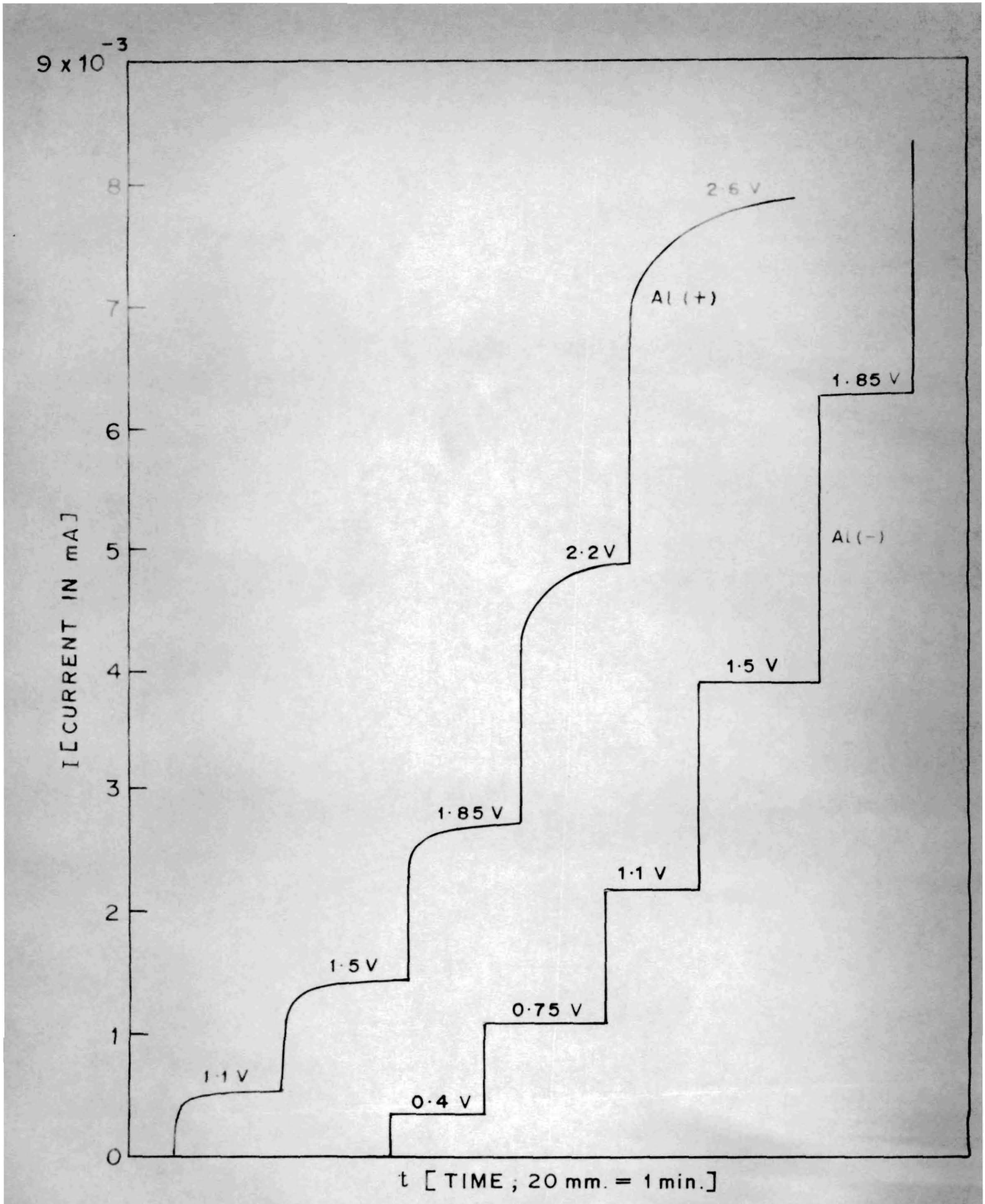


FIG. 3.17 RISE OF CURRENT WITH TIME IN CASE OF A Al-CdTe-Au SANDWICH (FOR THE TWO BIAS DIRECTIONS).

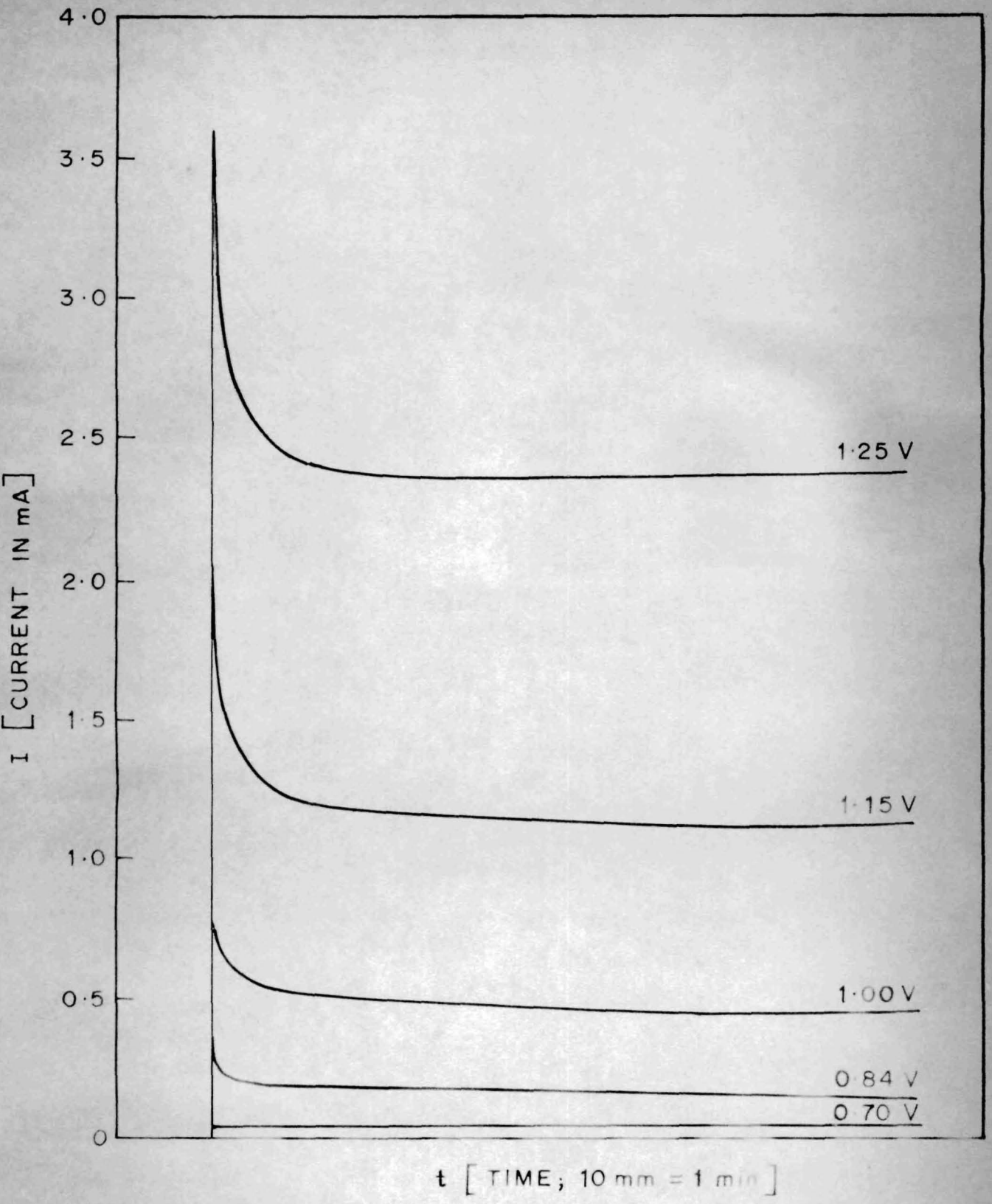


FIG. 3.18. DECAY OF CURRENT WITH TIME IN CASE OF A FORWARD BIASED Al-CdSe-Au SANDWICH (Al - POSITIVE)

At lower temperatures this effect remains, although there may be a small change in the time constant.

The fact that these time effects are not observed after formation clearly indicates that this dependence is connected with the formation process. In fact, the absence of time dependence could be taken as a sure test of "formation".

Slow rise as well as decay of current with time are well-known in case of metal-semiconductor rectifiers (Henisch[4]). Rise of current is commonly called "positive creep"and decay "negative creep". Both are often observed in the process of "formation" in rectifiers. It has also been found as in our case, that this effect is more pronounced for the reverse bias.

Henisch and Ewels[121] have found that the creep phenomenon is only slightly affected by temperature in case of selenium rectifiers. From -60° C to $+60^{\circ}$ C the effect is found to increase only slightly.

Cooper and Harrington[122] have shown that a rise of temperature is not necessarily associated with positive creep. The non-thermal character of positive creep can

also be concluded from the fact that application of comparatively low reverse voltage after the formation at high voltage results in a pronounced positive creep.

A some what similar relaxation phenomenon has been reported by several workers during studies on CdS. Hayashi[123] has reported a relaxation of current in single crystals of CdS. He has attributed the increase of current to the slow relaxation of surface states present in the insulating layer at the metal CdS interface.

Gershun[124,125] has also observed a slow formation of surface charge in a single crystal of CdS with deposited In electrodes. When a constant potential difference is applied to such a crystal, a counter e.m.f. has been observed as manifested by the fact that when the external source of voltage is switched off, a current flows in the circuit, in the direction opposite to the direction of the current flowing under the action of external applied voltage. The counter current decreases slowly with time. It has been found that the charge is independent of crystal thickness from which it has been concluded that the charge is not generated throughout the crystal but only in the surface layer whose thickness is approximately 1.2×10^{-5} cm. The accumulation of charge is associated with the capture of carriers. It is assumed that under external electric

field surface states are populated leading to the accumulation of charge on the surface of a crystal. When the applied voltage has been removed the charge is liberated from the surface levels and gives rise to a counter current.

Snow et al[126] have reported evidence of ion transport in insulating films, by studying capacitance-voltage characteristic of a metal-insulator-semiconductor system.

Adirovich et al[111] have studied relaxation phenomena in CdS thin film diodes prepared by vacuum deposition on hot substrates. Au, In, Al and Ag have been used as electrode materials with Au as base electrode. Au-CdS-Al sandwiches show a strong relaxation. On the other hand, Au-CdS-In diodes do not relax. The forward current (Al+) first rises to I_o and then decreases with time to I_s which is several per cent of I_o. When a particular voltage is applied, the drop in forward current first occurs rapidly and then more slowly. If the voltage is switched off and after some rest time, switched on again, the resulting current is less than the previous one.

They have also found that relaxation properties of the reverse biased diode depends sharply on the specific

resistance of the film. For the low resistance samples (10^5 - 10^6 ohm cm) the time dependence is complex. After rapid initial fall, the current begins to rise slowly. The increase of current lasts from tens of minutes to several hours. Comparison of the I-V characteristics of the diodes Au-CdS-In and Au-CdS-Al shows that a barrier layer arises at Al contact while there is no such layer on In. This has been proved by the fact that photovoltage arises on the Al side but not on In. They have concluded that the relaxation phenomena are related to the processes that take place in the barrier layer near the contact and are due to high voltage polarisation complicated by over charging of the traps. In contrast to the current drop, an increase of current, according to them is an extremely unusual phenomenon and till the time of their publication, they claim there are no observations similar to these. Increase in the reverse current observed in low resistive CdS films has been tentatively explained as due to the rearrangement in the space charge region during over charging of the traps leading to a decrease in the field near the contact.

3.3 PHOTOVOLTAIC AND PHOTOCONDUCTING PROPERTIES

3.3.1 PHOTOVOLTAIC PROPERTIES

Figure 3.19 shows the behaviour of the open circuit photovoltage as a function of time for a Al-CdSe-Au sandwich. It can be seen that on illumination, a photovoltage is developed with Al electrode positive and gold negative (forward direction). This sign of photovoltage is consistent with the existence of a barrier at the Al-nCdSe interface, a conclusion already arrived at on the basis of the I-V characteristics in dark. Furthermore, from figure 3.19, it can be seen that the photovoltage reaches a steady value under illumination in about a mimute. On switching off the light, the photovoltage first decreases sharply and then slowly attains zero value after mimutes.

The electron-hole pairs generated in the semiconductor region close to the barrier get separated due to the electric field present there. The electrons remain on the semiconductor side of the barrier whereas the holes move over to the side of the Al electrode. This results in the photovoltage with Al positive and Au negative as mentioned above.

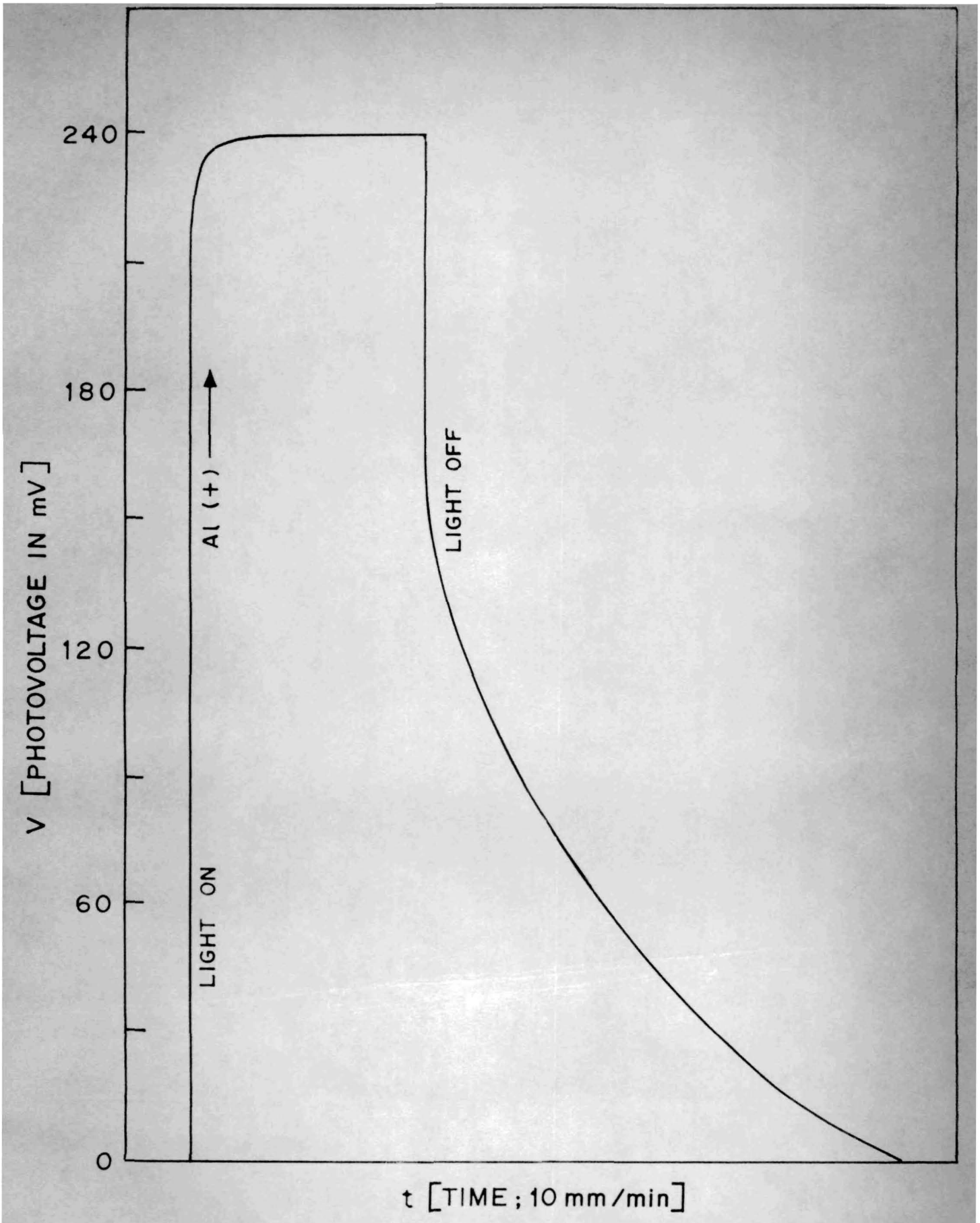


FIG. 3.19. VARIATION OF OF OPEN CIRCUIT ($R > 10^{12} \Omega$) PHOTOVOLTAGE WITH TIME IN A Al-CdSe-Au SANDWICH.

Sometimes, this type of photovoltage has been attributed to photoemission from the metal electrode (Williams and Bube[127]). For example, photons of sufficient energy absorbed in aluminium metal may cause a photoemission of electrons in the semiconductor across the barrier. This would lead to development of photovoltage of the same polarity as above. However, the following experimental results seem to rule out photoemission as the cause of photovoltage in our samples :

(a) The photovoltage is expected to reverse sign on changing the direction of illumination if it arises due to photoemission from the metal electrodes. No such reversal has been experimentally observed.

(b) The photovoltaic effect disappears on formation. If it was entirely due to the electrode, it would be difficult to explain its absence after formation.

(c) On this basis, it would be difficult to explain the temperature and voltage dependence of photoconductivity (to be described).

Thus, light absorption in the semiconductor and carrier separation by the barrier appears to be the proper explanation of the photovoltage.

The behaviour of the open circuit photovoltage as a function of time for Al-CdTe-Au sandwiches under illumination is shown in Fig. 3.20. First, a photovoltage is developed with Al electrode negative and Au electrode positive. The maximum value of this voltage is reached almost instantaneously. We call this as "maximum positive voltage V_m^+". While the illumination is still continuing, the voltage starts decreasing with time, becomes zero and finally changes its polarity. This decrease continues (i,e. the reverse voltage continues to increase in magnitude) with time and finally approaches a saturation value. We call this as "maximum negative voltage V_m^-".

If the light is switched off immediately after switching it on, i.e. before V_m^+ is attained, the photovoltage instantaneously falls to zero. If the light is switched off at a point after V_m^+ has been crossed but before V_m^- is reached, then the voltage first decreases instantaneously by a finite amount, then it increases gradually and finally reaches zero (see Fig. 3.20). If the light is switched off after the maximum steady value of V_m^- is reached, then also voltage first decreases instantaneously and then starts rising gradually and approaches zero after some time. Furthermore these sandwiches show some fatigue i.e. if light is switched on

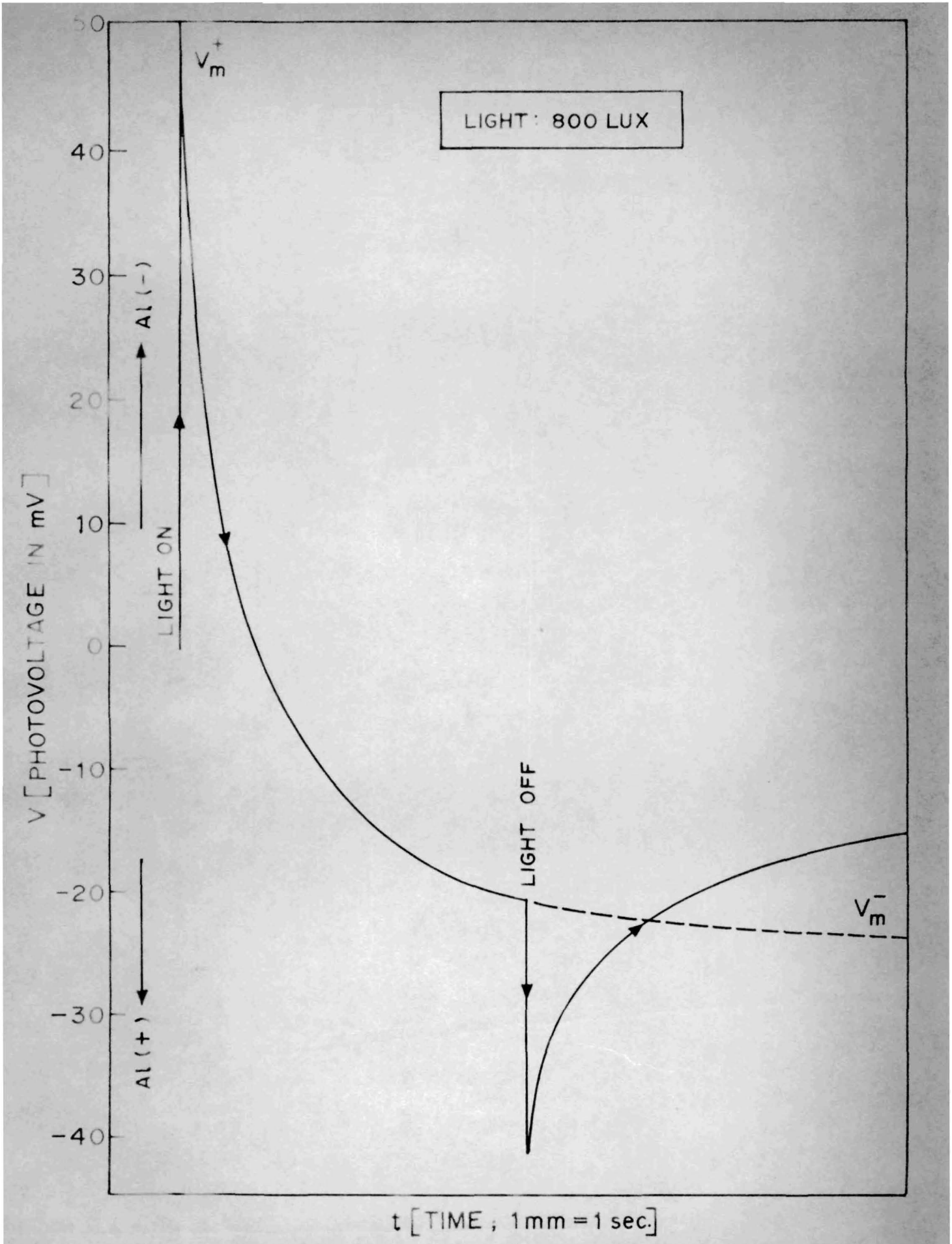


FIG. 3.20. VARIATION OF OPEN CIRCUIT ($R > 10^{12} \Omega$) PHOTOVOLTAGE WITH TIME IN A Al–CdTe–Au SANDWICH.

immediately after it has been switched off then the magnitude of the maximum voltage attained (V_m^+) would be smaller. To get the former high value of V_m^+, the sample has to be kept in dark for sufficiently long time before it is illuminated again.

The photovoltage-time dependence clearly points out to the existance of two photocells (let us call them A and B) connected in opposition and they have the following characteristics :

(a) The cell A developes negative voltage on the side of Al electrode and positive voltage on the Au side (forward direction for a rectifying CdTe). Furthermore, this cell responds to light very fast i.e. it attains its maximum voltage instantaneously on switching the light on and also the voltage drops to zero instantaneously on switching the light off.

(b) The cell B has the positive polarity on the side of the Al electrode and negative polarity on the side of the Au electrode. Its response to light is slow i.e. its voltage develops gradually under constant illumination and also falls off slowly after switching the light off. Furthermore, the ultimate voltage developed under constant illumination is greater for the cell B than for the cell A.

It can be easily seen that with a proper choice of the magnitude of the photovoltage and the response time of the two cells one can arrive at a resultant voltage-time graph fully matching with the experimental result. A similar analysis for the photovoltage reversal in thin films of Nb, Ta, Ti, Al-oxides sandwiched between Al and Au electrodes has been given by Chopra[128].

It now remains to identify these two photocells in the sandwich. In this connection, we may recall that while discussing the dark I-V characteristics we arrived at two possible explanations for the high resistance in both directions i.e. (i) high series resistance, or (ii) two barriers in opposition. The photovoltaic results just now described support the second conclusion.

3.3.ii PHOTOCONDUCTIVITY

As already discussed, the conductivity of the sandwich is increased markedly on illumination when it is reverse-biased (i.e. Al negative for CdSe, positive for CdTe, rectifying type). On the other hand, under forward bias (i.e. Al positive for CdSe and negative for CdTe) the per centage change in conductivity $\Delta\sigma/\sigma$ is not so marked because the dark conductivity itself is quite high. However, the non-rectifying type of CdTe sandwiches are photosensitive in both directions because of their low dark conductivity.

The response time (i.e. the time constant τ) varies from sample to sample, but in general it is approximately 8.5 m sec. for rectifying CdSe (Al-). CdTe sandwiches usually have lower time constant, 1.7 m sec. (Al+) and 0.8 m sec (Al-).

The interesting feature of this photoconductivity is its voltage dependence. A plot of log I_i vs $V^{1/4}$ of photocurrent for Al-CdTe-Au sandwich (non-rectifying type) with Al electrode positively biased is a straight line parallel to the log I_d vs $V^{1/4}$ where I_d is the current in dark and I_i is the current in presence of light (see Fig. 3.21). When Al electrode is biased negatively then we get a similar behaviour except for the fact that the plot of log I as a function of $V^{1/2}$ rather than $V^{1/4}$ gives a straight line for both photo and dark currents (Fig. 3.22).

Figures 3.23 and 3.24 show logarithm of photo-conductivity σ_i and dark conductivity σ_d as a function of temperature at a fixed applied voltage (2.5 v) and at constant illumination. One can observe a strong temperature dependence.

Furthermore the photocurrent does not rise linearly with the intensity of light. It tends to saturate at higher intensities.

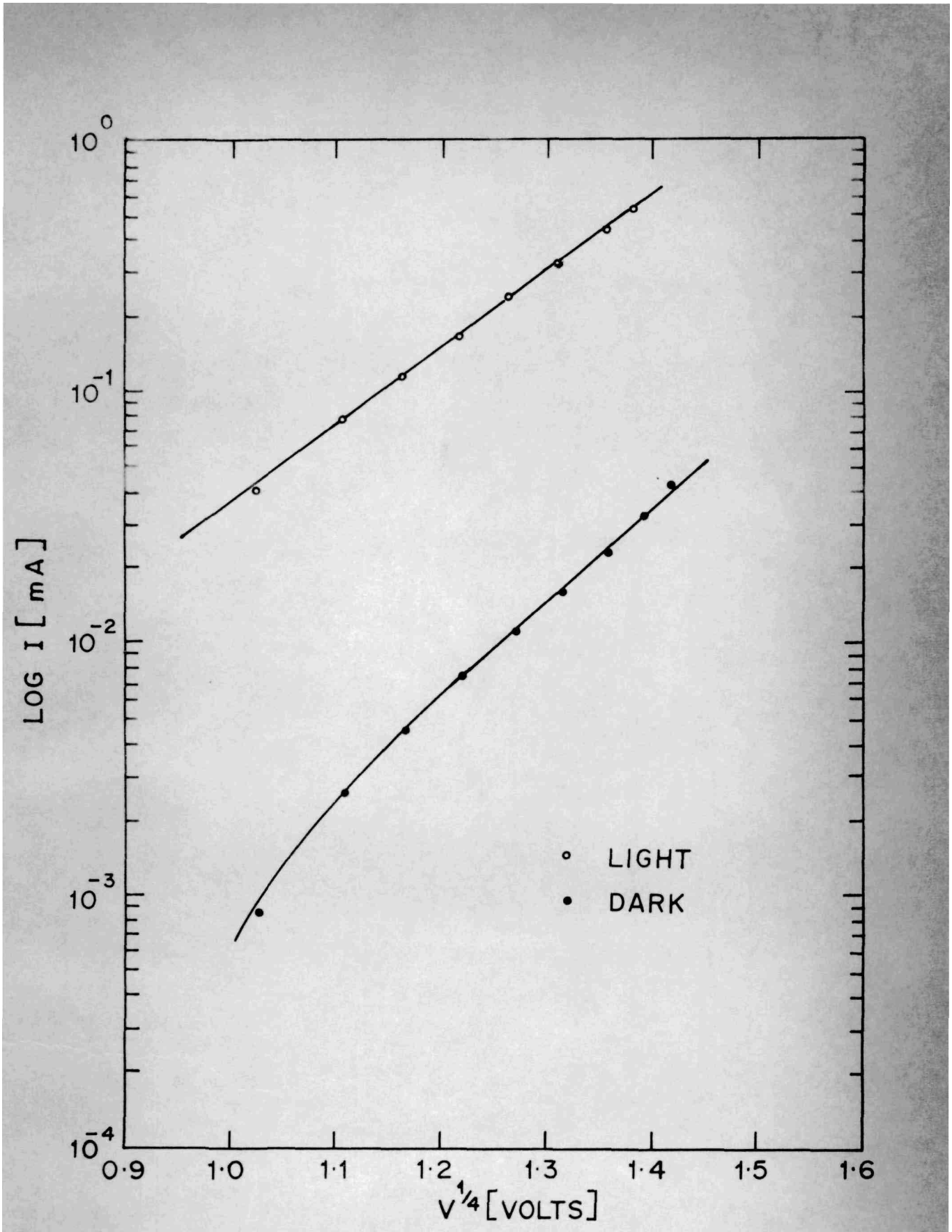


FIG. 3.21. LOG I VS $V^{1/4}$ CHARACTERISTIC OF A Al-CdTe-Au SANDWICH, ILLUMINATED AND IN DARK (Al POSITIVE).

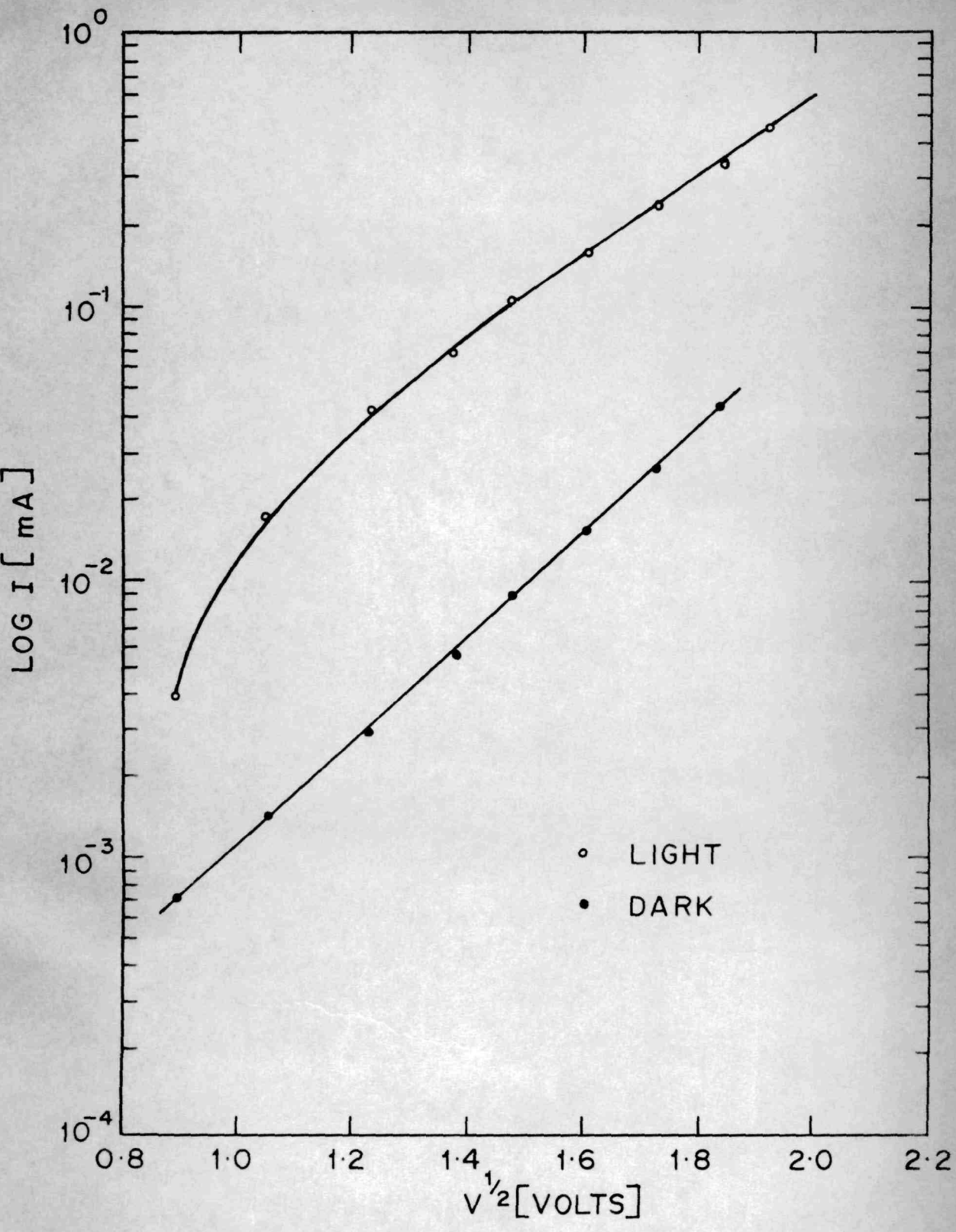


FIG. 3.22. LOG I VS $V^{1/2}$ CHARACTERISTIC OF A Al-CdTe-Au SANDWICH, ILLUMINATED AND IN DARK (Al NEGATIVE).

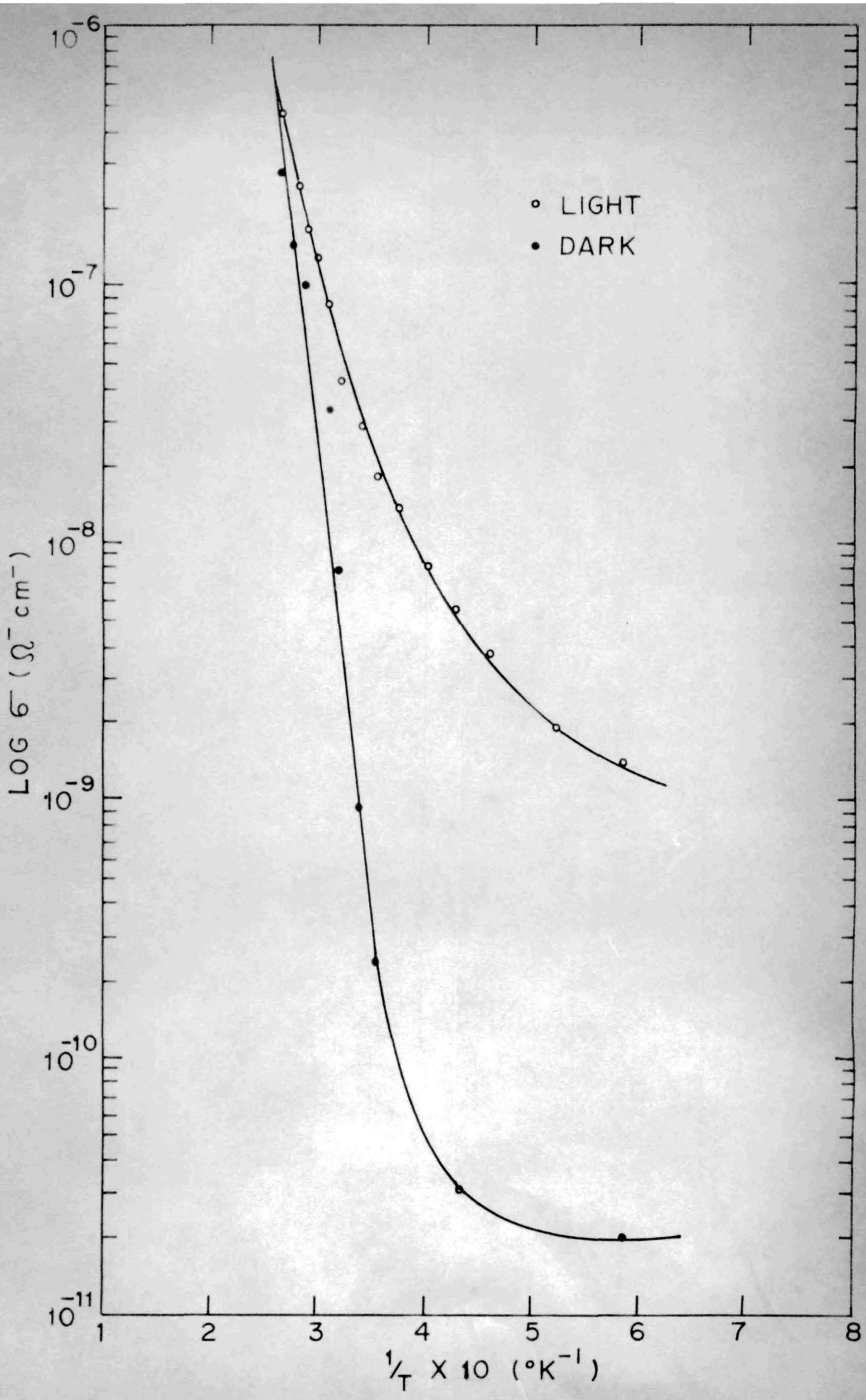


FIG. 3.23. LOG σ VS $1/T$ CHARACTERISTIC OF A Al-CdTe-Au SANDWICH, ILLUMINATED AND IN DARK (Al POSITIVE).

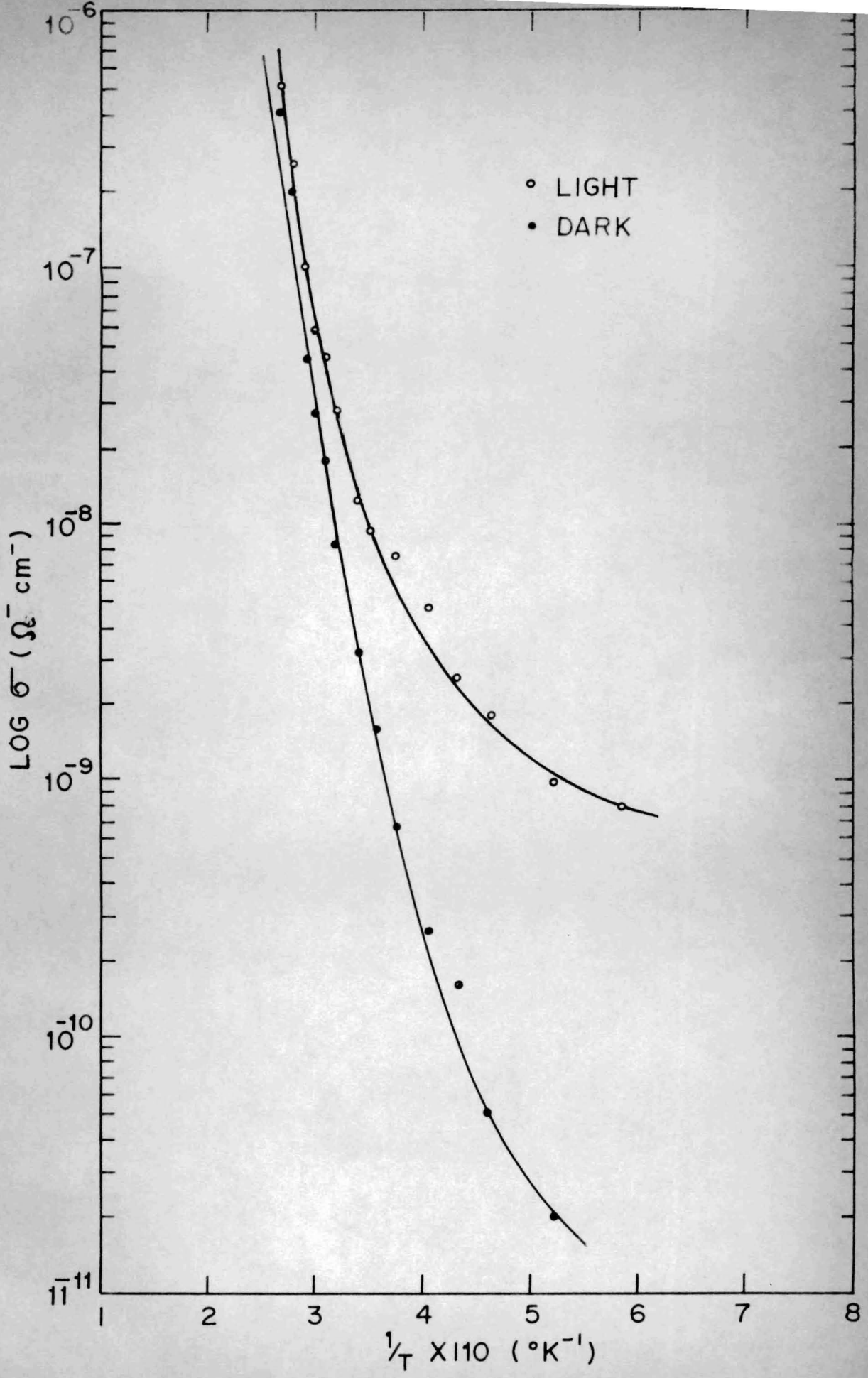


FIG. 3.24. LOG σ VS $1/T$ CHARACTERISTIC OF A Al-CdTe-Au SANDWICH, ILLUMINATED AND IN DARK (Al NEGATIVE

TABLE III

Dark conductivity σ_d and photoconductivity σ_i as a function of temperature for the sandwich B at 2.5 volts

$T^{o}K$	$1/Tx10^{3}K^{-1}$	σ_d ohm.$^{-1}$ cm^{-1}		σ_i ohm.$^{-1}$ cm^{-1}	
		Al(+)	Al(-)	Al(+)	Al(-)
171	5.85	2.0×10^{-11}	-	1.4×10^{-9}	8.0×10^{-10}
193	5.18	-	2.0×10^{-11}	1.9×10^{-9}	1.0×10^{-9}
217	4.60	-	5.0×10^{-11}	3.9×10^{-9}	1.8×10^{-9}
231	4.33	3.0×10^{-11}	1.6×10^{-10}	5.5×10^{-9}	2.6×10^{-9}
246	4.07	-	2.6×10^{-10}	8.0×10^{-9}	4.8×10^{-9}
260	3.76	-	6.8×10^{-10}	1.4×10^{-8}	7.8×10^{-9}
281	3.56	2.4×10^{-10}	1.6×10^{-9}	1.8×10^{-8}	9.2×10^{-9}
293	3.41	9.6×10^{-10}	3.2×10^{-9}	2.9×10^{-8}	1.2×10^{-8}
310.5	3.22	7.8×10^{-9}	8.2×10^{-9}	4.2×10^{-8}	2.8×10^{-8}
321.5	3.11	3.28×10^{-8}	1.8×10^{-8}	8.5×10^{-8}	4.3×10^{-8}
333	3.00	-	2.8×10^{-8}	1.3×10^{-7}	5.8×10^{-8}
345	2.90	1.0×10^{-7}	4.4×10^{-8}	1.7×10^{-7}	1.0×10^{-7}
355.5	2.81	1.4×10^{-7}	2.0×10^{-7}	2.4×10^{-7}	2.6×10^{-7}
377	2.65	2.8×10^{-7}	4.0×10^{-7}	4.6×10^{-7}	5.0×10^{-7}

Sample has 0.5/c electrode spacing and 0.1 cm^{2} area.

3.4 SWITCHING AND MEMORY PHENOMENA

3.4.1 GENERAL FEATURES

In the beginning of this chapter we have given the dynamic I-V behaviour of the observed switching phenomenon in Al-CdTe-Au and Al-CdSe-Au sandwiches and described their main characteristics. Now we give some more details relating to the post-formation stage where switching has been observed. Based on this a tentative mechanism for this unusual effect will be proposed.

Figure 3.25 shows a linear I-V plot of the low conductivity state of switching developed on the application of steady (D-C) voltage at liquid nitrogen temperature. High conductivity state i.e. ohmic part could not been displayed on this linear plot because of its high current values. Thus only switching voltage values are pointed out. It may be emphasised that here also the sample switches from low conductivity state to high conductivity state only when Al electrode is made negative. Any attempt to bring the sample again to low conductivity state either by increasing or by decreasing the voltage when Al electrode is negatively biased is unsuccessful. Furthermore, after keeping the voltage off for sufficiently long time (5 hours) the sample is still found to be in the

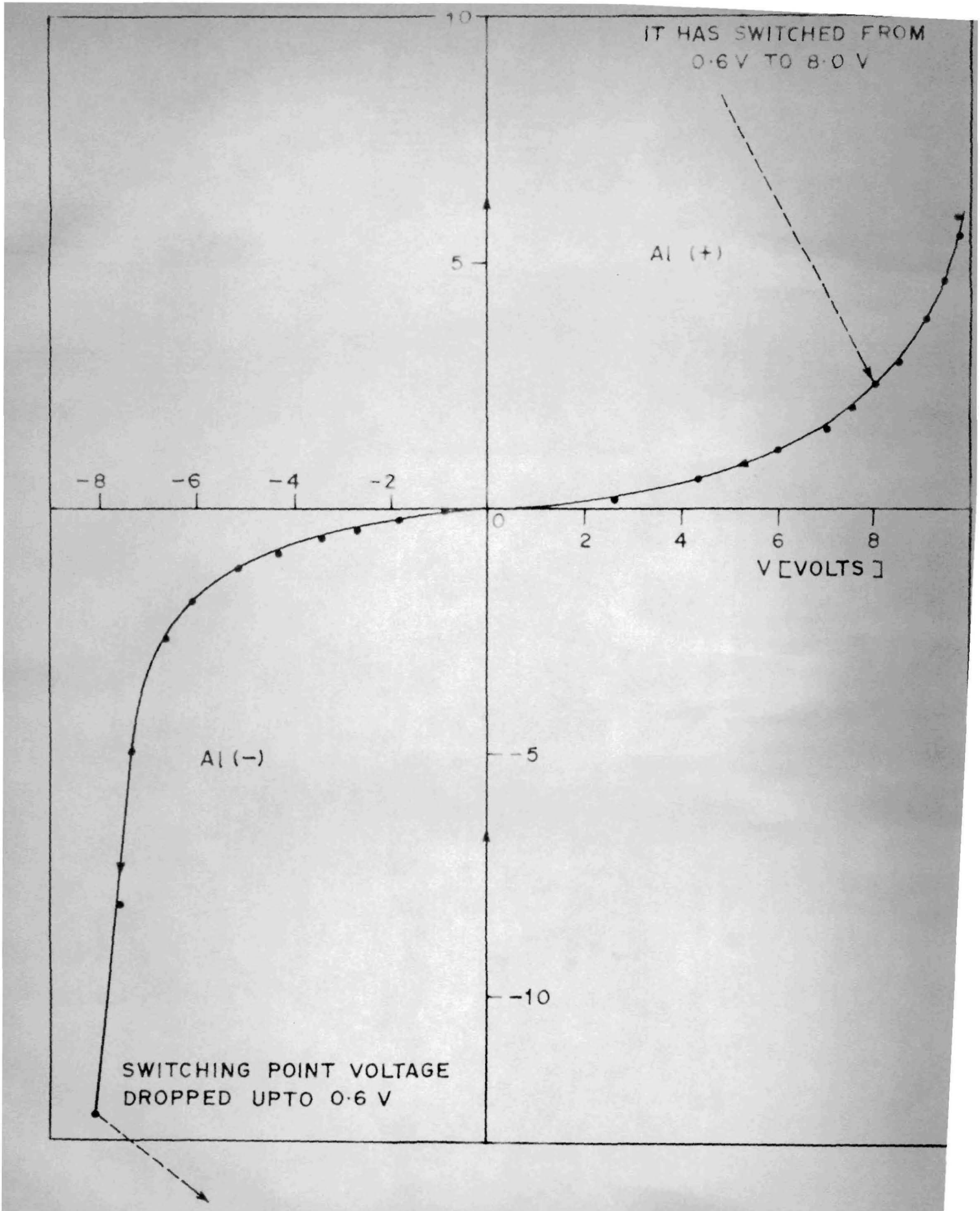


FIG. 3.25. STEADY STATE I-V CHARACTERISTIC OF THE LOW CONDUCTIVITY STATE IN AN Al-CdTe-Au SANDWICH WHICH HAS BEEN BROUGHT TO REVERSIBLE SWITCHING AT LIQUID N_2 TEMPERATURE.

original high conductivity state without any detectable change. However, when the polarity is changed by making Al positive, the sample switches back to low conductivity state at the threshold voltage of 0.6 v. In addition, this experiment which has been repeated many times proves that the formation and switching can take place even at liquid nitrogen temperature which rules out gold ions incorporation found by Simmons and Verderber[70] in their SiO sandwiches where switching could not be obtained below - 40° C. In the present study, on the contrary, switching is more stable at low temperatures since the sample is protected from the possible damage due to heating caused by power dissipation. Fig. 3.26 (a and b) shows plot of log J vs $V^{1/4}$ for Al(+) (reverse direction) and log J vs V for Al(-) (forward direction) of the low conductivity state given in Fig. 3.25. Fairly straight lines in these figures undoubtedly show that the mechanism of conduction is more or less the same in post- and pre-formation stages especially in low voltage range. However departure from linearity at higher voltages makes this problem a bit complex. Because of this, it is rather difficult to distinguish preformation from postformation stage. In general, a sample of a rectifier like I-V behaviour loses to some extent, its high reverse resistance after such formation.

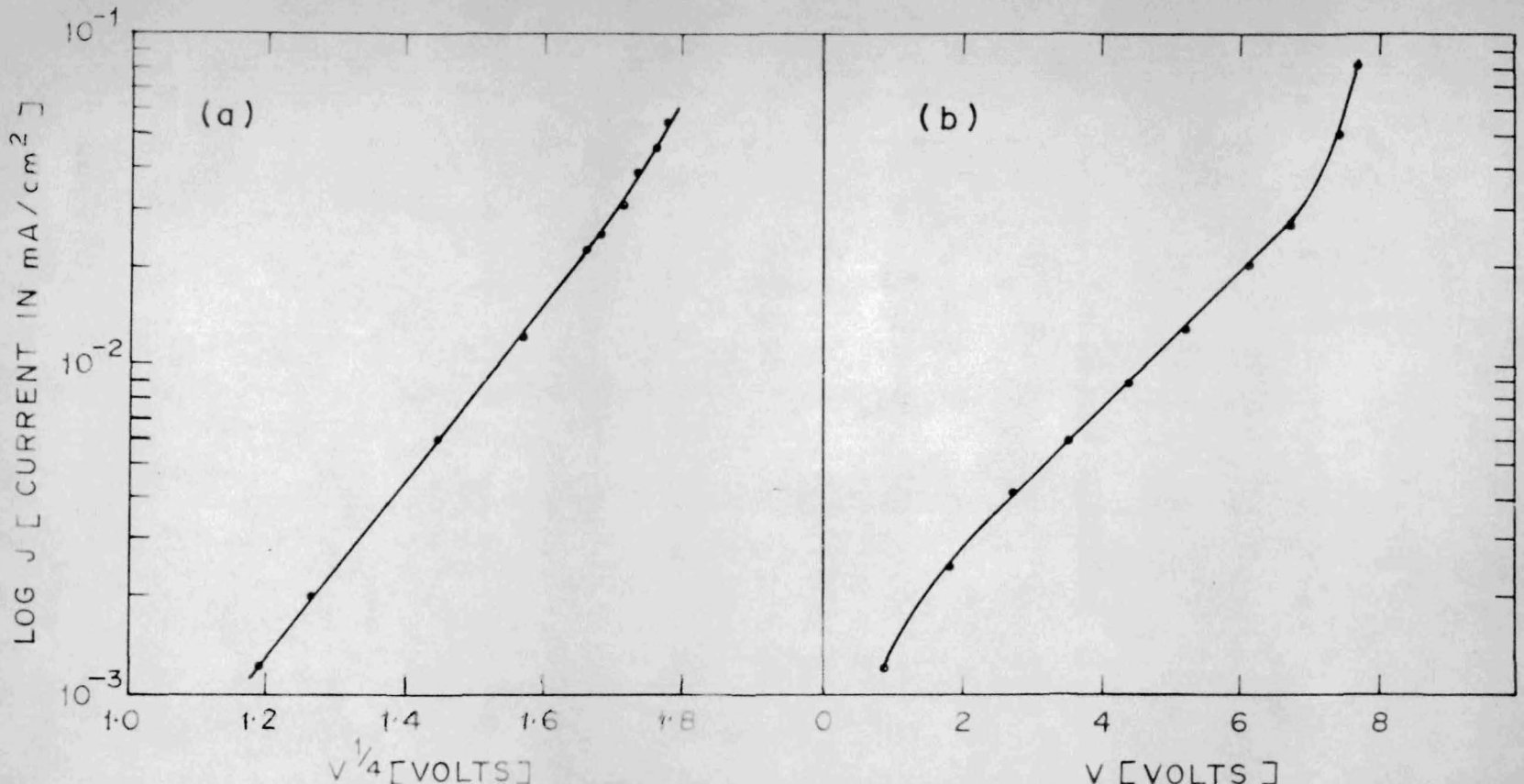


FIG. 3.26. LOG J VS $V^{1/4}$ (a) AND LOG J VS V (b) CHARACTERISTICS OF THE LOW CONDUCTIVITY STATE GIVEN IN FIG. 3.25.
(a) Al POSITIVE, (b) Al NEGATIVE.

The amount of increase in conductivity varies from sample to sample and if this is small, the sample preserves high resistance and photosensitivity i.e. there will not be any significant difference between the I-V characteristic of a virgin sample and that of the low conductivity state of the same sample after switching is established. This is the best shown in Fig. 3.27 (i,ii,iii). These photographs are from the sample A, of which the log J/T^2 vs $1/T$ and log J vs $V^{1/4}$ results have been already discussed (see page 98 and Fig. 3.9, 3.10, 3.11, 3.12, 3.13). Fig. 3.27(i) shows the I-V behaviour of the virgin sample in dark and under illumination at room temperature before temperature measurements have been taken. Fig..(ii) exhibits excellent switching (developed after temperature measurements have been completed and sample cooled down to room temperature) produced by applying sufficiently high negative voltage on Al electrode. After taking this photograph the voltage has been reduced below the threshold switching voltage with the sample in low conductivity state and photograph iii has been taken (in dark and under illumination). This figure shows that rectification as well as photosensitivity have been preserved even after formation.

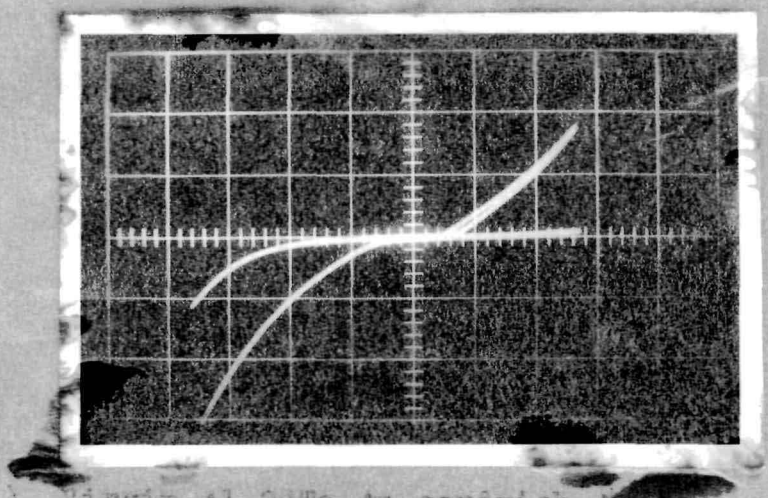


Fig. 3.27 (i) Virgin Al-CdTe-Au sandwich at room temperature in dark and under light. Horizontal : 10 v = 8 divs. Vertical : 0.11 mA = 1 div. Applied frequency 0.25 Hz

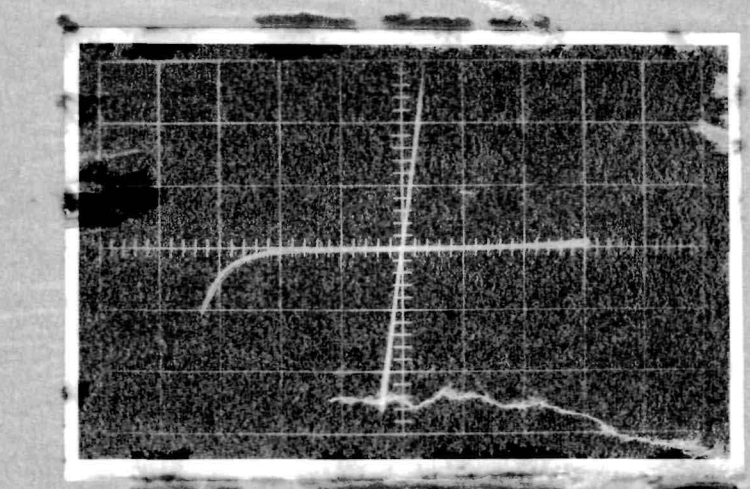


Fig. 3.27 (ii) Switching phenomenon at room temperature in dark. Horizontal : 10 v = 4.6 divs. Vertical : 5.5 mA = 1 div. Applied frequency 0.25 Hz.

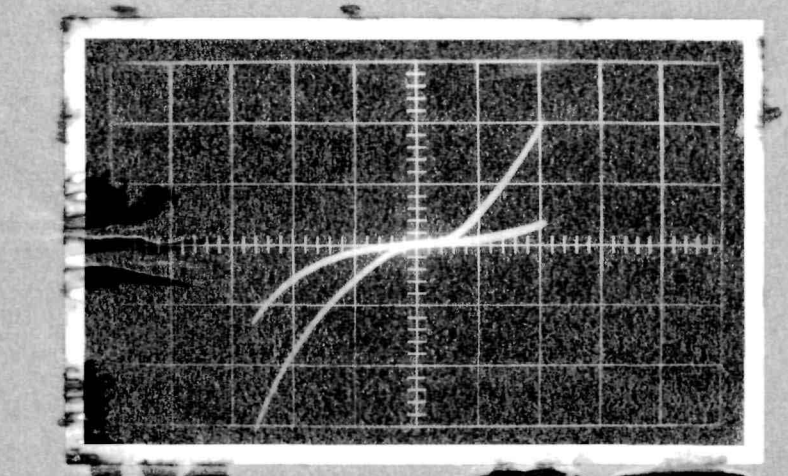


Fig. 3.27 (iii) At room temperature, under a voltage less than that required for switching, in dark and under light. Horizontal : 10 v = 8 divs.
Vertical : 0.037 mA = 1 div.
Applied frequency 0.25 Hz.

The dependence of switching voltage on temperature has also been studied. It is found that the effect of temperature in the postformation stage depends mainly on the extent of "formation". Samples which have not lost their virgin characteristics will apparently preserve their high temperature sensitivity which is so typical of the unformed samples. On the other hand, high conductivity ohmic state remains temperature insensitive for all types of sample. Fig. 3.28 (a, b, c, d) gives the four I-V curves taken under applied voltage of 0.25 Hz, all of which show switching. Curves a, b, c and d correspond to room temperature, - 15°, - 45° and - 120° C respectively, from where it is clear that the threshold voltage increases with decreasing temperature. On increasing the temperature from - 120° C to 150° C the threshold voltage decreases from 9 volts to 5 volts.

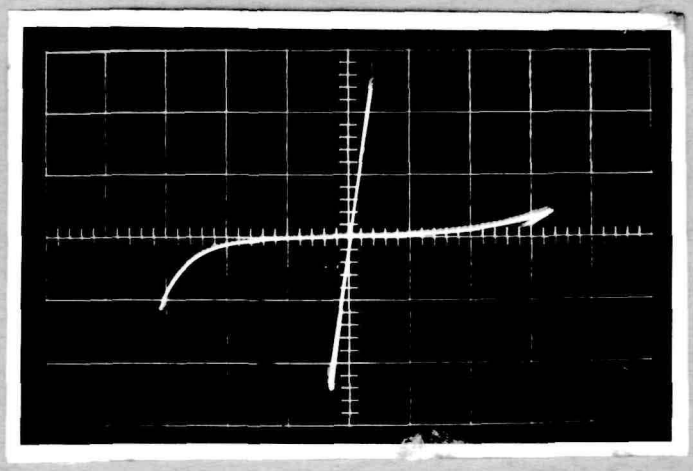
Here it is worthwhile mentioning that sometimes the sample which is not fully formed may show negative dJ/dT in the low conductivity part of the switching state at temperatures below room temperature. However, above room temperatures the current at any given voltage rises on increasing temperature.

We have already mentioned that the low conductivity part of the switching state has generally a higher

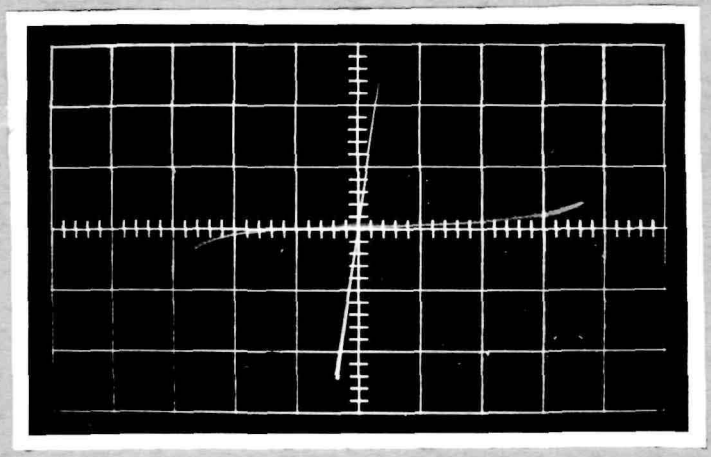
Fig. 3.28 Al-CdTe-Au sandwich showing the switching phenomenon in dark.
Horizontal : 10 v = 5 divs.
Vertical : 5.5 mA = 1 div.
Applied frequency 0.25 Hz.

(a) Room temperature (b) - 15° C.

(c) - 45° C. (d) - 120° C.



(a)



(b).

conductivity than that of the virgin sample. Negative dJ/dT could be attributed to the slow reversal of the "formation" which appears in samples where virgin characteristics are slowly regained after switching.

Negative dJ/dT is a known effect in rectifiers and it has been reported by many authors in their study on selenium rectifiers. The effect has been attributed to processes responsible for formation, which in fact are not fully understood yet, or to thermal instability, or both.

3.4.ii HIGH FREQUENCY AND PULSED MEASUREMENTS

The dynamic I-V characteristics so far discussed have been obtained at a frequency of 0.25 Hz. The I-V behaviour has been studied under higher frequency also (upto 2500 Hz). At high frequencies the virgin sample shows a large phase shift of current with respect to voltage. This indicates a large RC time constant of the sandwich. This shift is much smaller in post-formation low conductivity state and is completely absent in the post-formation high conductivity ohmic state.

Pulsed voltage-current characteristic of the sandwiches have been obtained by applying rectangular pulses of 1 μsec duration and a repetition frequency of 1350 pulses/sec. The current voltage values have been observed on the oscilloscope.

Fig. 3.29 shows the (I-V) plot for an Al-CdSe-Au and an Al-CdTe-Au sandwich. The plots are more or less straight lines. From the slope of these graphs the resistance appears to be 130 ohms for CdSe sandwich and 200 ohms for CdTe sandwich. It may be mentioned that the resistance of these samples before pulse has been applied is : CdSe Al(+) 2.6 kilo-ohms, Al(-) 30 kilo-ohms and CdTe Al(+) 170 kilo-ohms, Al(-) 50 kilo-ohms . However as soon as the pulse is removed, the sample comes back to this original state. It is also interesting to point out that such a developed high conductivity ohmic state having the resistance of the above is not much different in values to that one which exists in cyclic switching (10-50 ohms).

3.4.iii FORMATION

Formation process has been reported by several workers in many thin film metal-insulator-metal samples. Verderber et al[71] have made a detailed study of the forming process in evaporated SiO thin films. However, there are some significant differences between the present observation and the earlier ones :

(a) To ratio of the resistance of the unformed sample to that of the formed sample (high resistance state) is between 1:1 to 100:1 whereas the earlier reported values are of the order of 10^8 : 1.

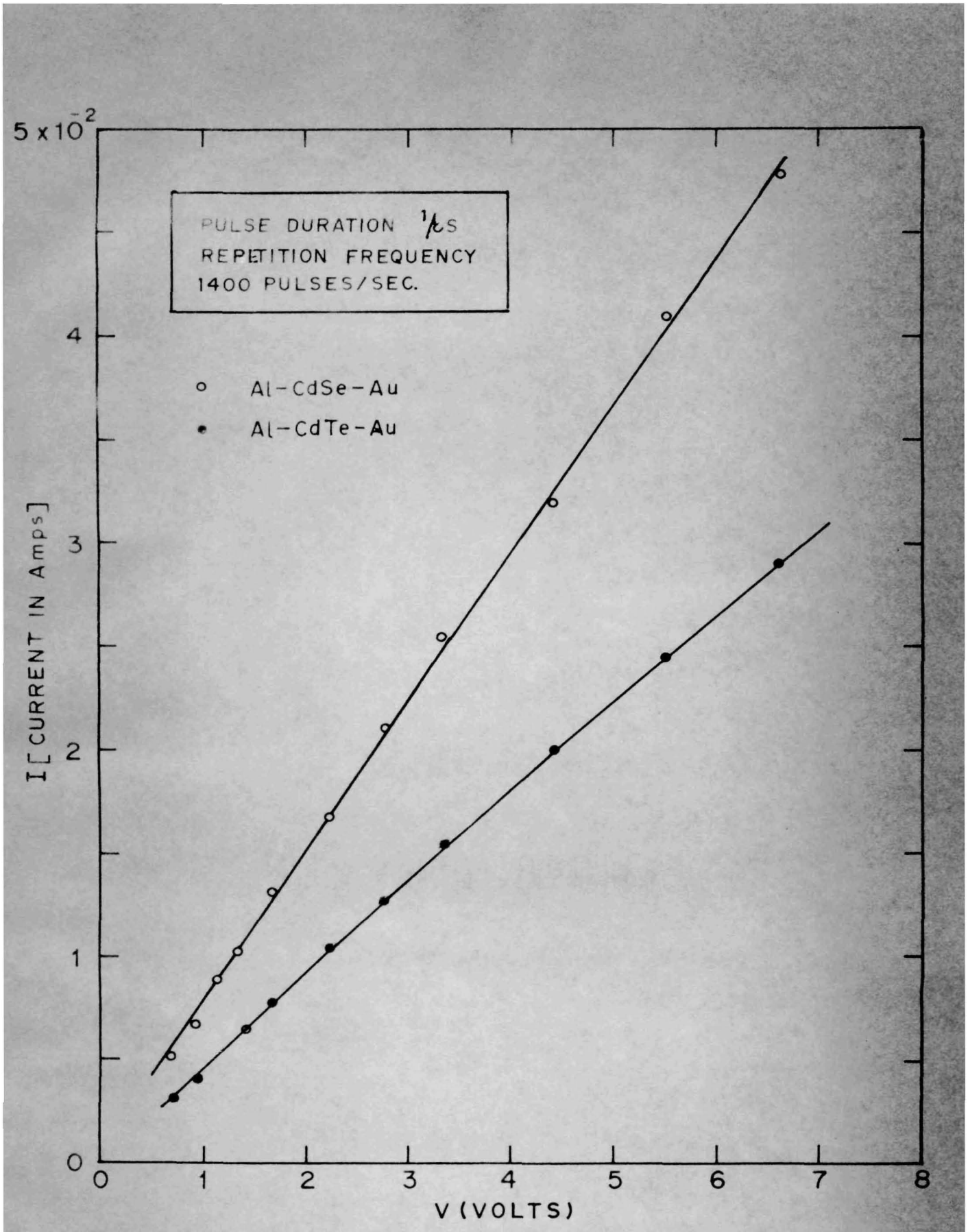


FIG. 3.29. PULSED I-V CHARACTERISTIC OF Al-CdSe-Au AND Al-CdTe-Au SANDWICHES.

(b) The samples could be formed with equal ease at liquid N_2 temperature as at room temperature or above it.

(c) The time taken for the formation in SiO films[71] is reported as 10 secs. at room temperature and more than an hour at - 40° C. In the present case the formation appears to be instantaneous.

It may further be pointed out that :

(1) For formation it is absolutely essential to make Au positive and Al negative.

(2) On formation, the first state to appear is the ohmic low resistance state. On the reversal, this switches to the high resistance state, but generally this resistance is less than that of the unformed sample.

(3) Those samples whose resistance is not very high in the unformed state cannot be formed to the bistable state. For example, Al-CdTe-Au sandwiches of the rectifying type where negative voltage on the Al electrode biases the sample in the forward direction causing a high current to flow at low voltages, cannot be brought to the switching state because the voltage across the sample does not reach the critical voltage. This brings to light the fact that 'switching' requires a certain threshold voltage and not a threshold current.

3.4.iv MEMORY

The most striking feature of these samples is the "memory" phenomenon. It is hardly necessary to emphasise that these structures are exhibiting the genuine "memory" effect in view of the fact that they can be brought to any of the two bistable conductivity states, where they remain permanently after removal of the voltage. Furthermore, the other not less important feature, is that the sample can be brought in one or the other conductivity state only after applying the threshold voltage of a particular sign. Therefore, one can speak of a "memory effect" which memories the sign of the applied threshold voltage. Furthermore, the ratio of the resistance in the high and low resistance states is very large indeed and also the conductivity in the low resistance state is ohmic. The associated photo effects make these structures still more interesting.

To our knowledge only three reports of a memory of this type exist : Patil and Sinha[68] (1967), Simmons and Verderber[70] (1967) and Ovshinsky[76] (1968). Patil and Sinha who have studied the Al-CdS-Al system have observed a similar switching and memory but in those samples (i) the switching from one state to another is much slower, (ii) the low resistance state is not ohmic,

(iii) the ratio of the resistance in the high and low resistance states is not as high as in the present case and (iv) no photoeffects are observed.

The samples prepared by Simmons and Verderber can show memory only under certain very special conditions i.e. when the applied voltage, after going through the negative resistance, is reduced to zero in less than 0.1 ms. Furthermore, the behaviour is symmetrical with respect to the applied voltage so that either polarity can induce the same state and thus the sample is not capable of remembering the polarity of the applied voltage. No photoeffects have been observed either.

After the present work has been completed, and a preliminary note already published [Antic and Sinha[79] (July 1968)], Ovshinsky[76] (November 1968) published a paper on the reversible electrical switching in amorphous semiconductor materials where he briefly mentions that his structures show "memory" effect. However, his structures are symmetrical and the switching behaviour is also symmetrical. It does not depend on the direction of the applied voltage. Furthermore, although the transition from low to the high conducting state takes place at a threshold voltage, the switching from high to low conducting state takes place on application of a high current pulse.

3.5 MECHANISM

Even a superficial examination of the present results is enough to show how complex the processes responsible for switching and memory might be. The phenomenon of negative resistance by itself is quite complex and it is not surprising to find that although so many alternative explanations have been put forward in past, none of them appears to be wholly satisfactory. The switching and memory make the process still more difficult to interpret. It is, therefore, only natural to expect that the model we choose to explain all our experimental results might not be unique and there could be other alternative possibilities.

Our experimental results have undoubtedly established the existence of a barrier in the virgin samples. The barrier is also present in the high resistivity state after reversible switching has been established. On the other hand, this is clearly absent in the high conductivity ohmic state. Thus, for reversible switching, we look for a mechanism which involves the alternate removal and formation of the barrier under alternating applied field.

Furthermore, it has also been established that the barrier is present close to the Al electrode. However,

it is desirable to know more about the nature of this barrier in order to find out the way in which it can be formed or removed.

In this regard some meaningful general observations might be mentioned. (i) This type of switching has been observed for three different semiconductors viz. CdS[68], CdSe and CdTe. It is, therefore, likely that any mechanism which makes use of any specific property restricted to a particular semiconductor would not hold. (ii) The presence of one Al electrode appears vital. It is also necessary that there be a short exposure to oxygen in between the deposition of Al and the semiconductor. It is reasonable to expect that other metals which can form similar oxide skin might also show switching. (iii) The establishment of high conductivity state takes place only when Al is made negative and Au positive, irrespective of the 'p' or 'n' character of the semiconductor. Thus the switching from low to high conductivity state or vice versa has nothing to do with the reverse or forward biasing of the diode but is intimately connected with the application of a voltage of a certain magnitude and polarity across the surface layer adjacent to the Al electrode.

In order to arrive at a model which would be able to cover all the experimental observations and results too, let us start from the high conductivity ohmic state.

As the specific resistance (ρ_0) in this state is of the order 10^3 - 10^4 ohm cm., it is likely that there is a high impurity concentration in the sandwiched semiconductor, leading to a nearly degenerate case. The energy band diagram for such a sandwich is given in Fig. 3.30 (a) for n-CdSe and in Fig. 3.30 (c) for p-CdTe. The sandwiches switch from this state to the high resistive one (i.e. the barrier is formed) on applying a small (0.5 - 0.7 v) positive voltage on the Al electrode.

In the case of CdSe electrons (majority carriers) will flow from the semiconductor to the Al electrode which is made positive. As soon as a certain threshold voltage is reached, it is believed that the electrons get trapped in the region between Al and the semiconductor surface i.e. they remain bound there. Equal positive charge is created in adjacent semiconductor surface due to ionised donors. Such a model, viewed from semiconductor side will show that the conduction band is bent upwards as in the case of conventional n-type semiconductor at the blocking contact. This leads to the formation of a barrier at Al-semiconductor interface as shown in Fig. 3.30 b. As soon as the barrier is formed the sample switches over to the high resistance state and the current falls. Further, increase in the positive voltage on the Al electrode would lead to an increase in current as in a forward biased diode which

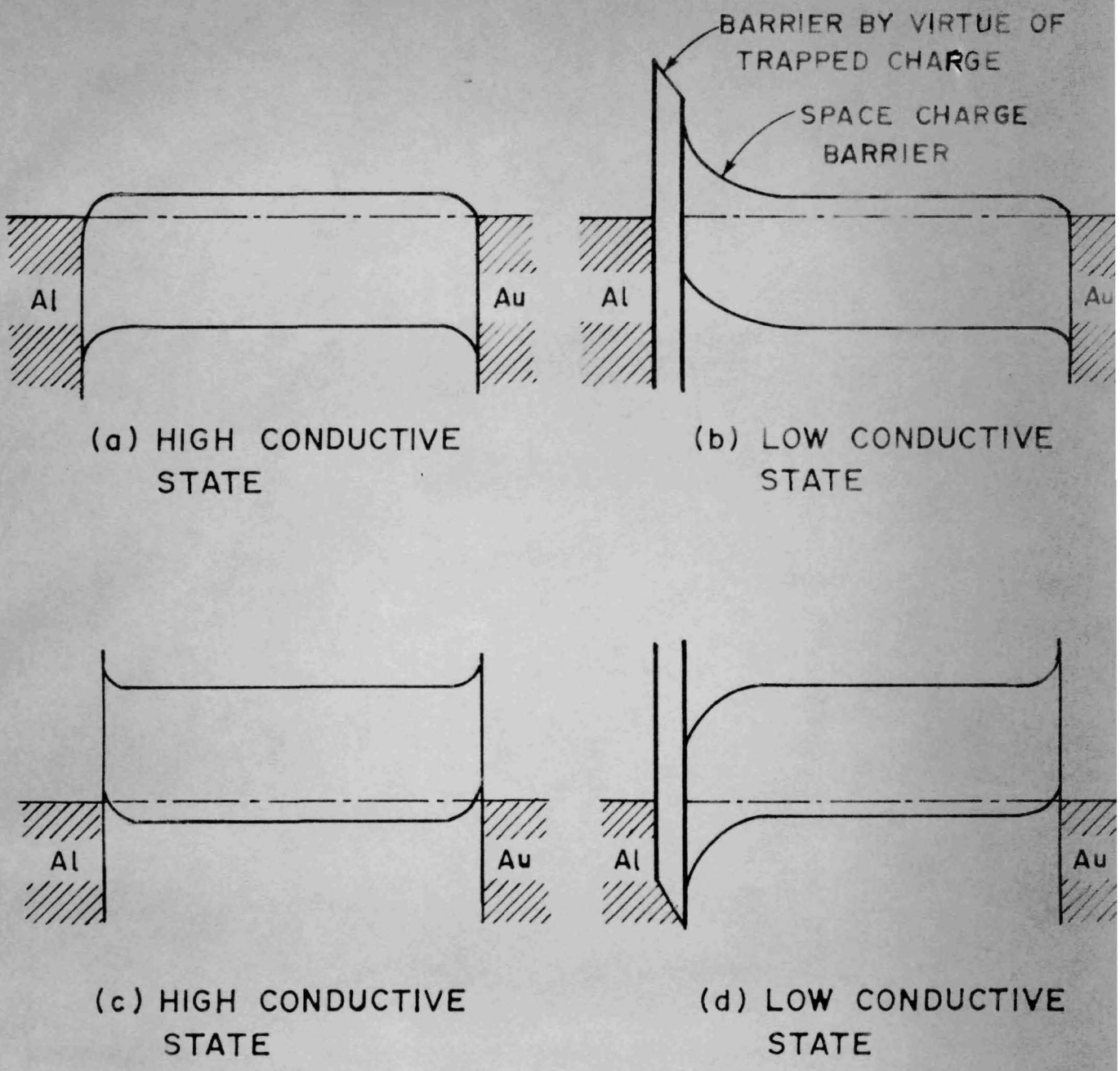


FIG. 3.30. BAND DIAGRAM FOR TWO CONDUCTIVE STATES (a) AND (b) CdSe ; (c) AND (d) CdTe

has actually been observed in the results presented earlier. The log J vs V plot is a straight line supporting the diode-like characteristic. On decreasing the voltage the diode behaviour is still maintained because the trapped carriers are not released as long as the polarity remains unchanged. The positive voltage on the Al electrode keeps the electrons bound to the centre close to it while the positive charge remains bound on the semiconductor side.

On making Al negative the sandwich remains in the high resistance diodic state. This direction of applied voltage should bias the sandwich in the reverse direction. In fact, the experimental I-V characteristic is also that of a reverse biased diode for this direction of the applied voltage. Log J vs $V^{1/4}$ is a straight line as is required for a reverse biased diode subject to barrier modulation by image force (Schottky field emission). If one keeps on increasing the negative voltage on the Al electrode the sandwich switches to the former high conductivity ohmic state at a certain threshold voltage (8-10 volts). This leads us to the conclusion that the double layer formed by trapping of electrons which happens due to the very specific nature of the interface between the metal and the semiconductor, gets shorted by applying large negative voltage on the Al electrode. If one imagines that this double

layer acts as a sort of a capacitor, it is natural to expect that such a thin capicitor will get discharged on applying a high voltage of appropriate sign. In other words it is assumed that the trapped electrons will get released and neutralise the positive charge on the semiconductor which has been induced there only by the existence of the negative charge in the trapping centre. However, if the reverse resistance is small i.e. the reverse current is large the switching will never take place since a sufficiently high field is not created. It is, therefore, believed that the entire diode characteristic is governed by the ability of this specific thin layer interface between the metal and the semiconductor to capture and trap the electrons. If this ability is poor, the barrier will be small and sample will have poor diode-characteristics.

Additional support for this proposed model comes from the observed results on pulse measurements. The sandwich with the barrier and having resistance of $10^4 - 10^5$ ohms. shows a resistance of only 10^2 ohms under the pulse. After removal of the applied pulse the sample is found to be again in the high resistive state without any detectable change. This proves that there exists a condenser in parallel to the high resistance of the sandwich which gets shorted at high frequency. In other words the

main resistance arises from the double layer in the barrier which also acts as a capacitor.

The sample can therefore be represented by two resistors in series one due to the film of $R_1 \sim 10^2$ ohms and the other due to the barrier $R_2 \sim 10^5$ ohms. In addition there is a capacitor in parallel to the high barrier resistance element, which gets shorted at high frequencies. There is also a switch in parallel to this resistor which opens when Al is positive and closes when Al is negative.

The opening and closing of the switch has just now been attributed to formation and removal of the barrier by trapping and detrapping of charged carriers respectively. There are, however, other plausible ways in which opening and closing of this switch can be governed by the polarity of the applied field.

It is well-known that the ionised impurities within the barrier region are in a strong electric field which tends to move them towards the metal electrode. This tendency is further enhanced by the application of negative voltage on the Al electrode. The positively charged centres move towards the metal electrode either by electron "hopping" or by ionic migration and at a certain threshold field the barrier becomes so thin that the charge carriers can cross it by tunneling. This would

amount to switching from a diodic state to ohmic conducting state. The difference between this model and the previous one is that in this case the charged double layer is not neutralised. There is only a redistribution of space charge making the barrier very thin and transparent to the charge carriers. In the previous model, however, there was a neutralisation of the double layer and a complete removal of the barrier.

This thin barrier remains stable even after the removal of the field and changes back to the thick barrier only on application of the reverse field. Thus there are two stable space charge distributions : (a) which leads to a wide blocking barrier and (b) which leads to a thin transparent barrier. Both these distributions are equally stable at zero field but at a certain negative voltage on Al, distribution (b) is stabilised as compared to (a) and vice versa for the reverse field. Two stable distributions at zero field are rendered possible because of the special nature of the interface between the metal and the semiconductor. However, it appears impossible to make any further conclusions about the nature of such a layer in view of the limited data at our disposal. It is, however, believed that to some extent, ionic process at this interface might be responsible for this distribution.

A third possibility is the alternate creation and destruction of a conducting path across the barrier. This could result from the alternate precipitation and dissolution of metal ions from the electrode material in the barrier region under the action of the appropriate field. The precipitation of metal ions would lead to a band formation in the forbidden band and would offer a conducting path across the barrier. The removal of these by the application of the reverse field would remove the band and re-establish the blocking barrier. A similar mechanism is believed to hold for flexodes fabricated by Kessler and Tompkins[63]. However, in this device it was necessary to heat it to 100° C to establish the conducting path. This is not so in our case where the switching can be had even at - 200° C. This process therefore may be difficult to justify in our case unless one assumes that there is some local heating.

Once the existence of barrier in virgin sample is established, there appears to be no difficulty in explaining the observed photo effects.

If a CdSe sandwich (open-circuit) having the band diagram given in figure 3.30 (b) is illuminated, the electron-hole pairs generated in the semiconductor region close to barrier, get separated due to electric field

present there. The electrons remain on the semiconductor side of the barrier whereas the holes move to the Al electrode. As can be seen from figure holes do not experience any barrier which will prevent their collection at Al electrode. As a result, a voltage difference will be created across the sandwich with the same polarity as that which gives a forward bias to the sandwich (Al+), (Au-) which is usual with any conventional photovoltaic cell.

Photovoltage-time dependence given in Fig. 3.19 shows how on switching the light on, the voltage assumes its constant value instantaneously, and how it decays first rapidly and then somewhat slowly after the illumination has ceased. The slow decay of photovoltage could be explained on the basis of the slow release of carriers from the trap centers. This brings out the fact that some of the photo-generated carriers get trapped and are released only slowly on switching the light off. It is likely that these trap centers are located in the interfacial layer where we envisaged the initial capture of electrons to establish a barrier.

The observed photovoltage is undoubtedly another fact which speaks in favour of the proposed barrier diagram. It also appears possible to explain the observations in regard to the photoconductivity measurements on the basis

of the above concepts, i.e. the existence of a barrier at the Al-CdSe interface. One can see that our CdSe sandwich acts as a photodiode. Under reverse bias, the photo-generated electrons move to the positive Au electrode and holes to the negative Al electrode. Neither of these experience any barrier. When the polarity is changed (forward bias) there will not be any significant difference between the current in dark and under illumination because of the low resistance. In addition, it is believed that the photoconductivity in this case is also governed by the lowering of the barrier at the metal-semiconductor interface in presence of light[129,130].

At this stage it may be worthwhile discussing the nature of the "formation" process observed in these sandwiches. This "formation" as already mentioned is associated with the (i) decrease in the resistance, (ii) loss of slow relaxation effects and (iii) loss of photoconductivity and photovoltaic properties. It may be recalled that the "formation" is observed after the first cycle of switching is completed when it is found that the sample does not come back to the original resistance of the virgin state.

This clearly indicates that the changes taking place in the first switching from the virgin to high conductivity ohmic state is not completely reversed on

of the above concepts, i.e. the existence of a barrier at the Al-CdSe interface. One can see that our CdSe sandwich acts as a photodiode. Under reverse bias, the photo-generated electrons move to the positive Au electrode and holes to the negative Al electrode. Neither of these experience any barrier. When the polarity is changed (forward bias) there will not be any significant difference between the current in dark and under illumination because of the low resistance. In addition, it is believed that the photoconductivity in this case is also governed by the lowering of the barrier at the metal-semiconductor interface in presence of light[129,130].

At this stage it may be worthwhile discussing the nature of the "formation" process observed in these sandwiches. This "formation" as already mentioned is associated with the (i) decrease in the resistance, (ii) loss of slow relaxation effects and (iii) loss of photoconductivity and photovoltaic properties. It may be recalled that the "formation" is observed after the first cycle of switching is completed when it is found that the sample does not come back to the original resistance of the virgin state.

This clearly indicates that the changes taking place in the first switching from the virgin to high conductivity ohmic state is not completely reversed on

reverse switching. In other words, the removal of the barrier in the virgin sample is partially reversible and partially irreversible. The "irreversible" part is due to certain labile positively charged centers which move towards the aluminium electrode during the first switching and remain stabilized in a narrower barrier region.

The time dependence of current in the virgin sample also appears to be due to a slow migration and readjustment of the labile charged centers in the space charge region under the applied field. For reverse bias, the type of double layer shown in Fig. 3.30 (b) is subjected to a field which tends to draw the positively charged centers towards the Al electrode making the barrier thinner. The current in presence of a thinner barrier is obviously higher so that a slow increase of current is observed under a constant applied field.

Under forward bias the field is reversed so the migration of the charged centers takes place in the opposite direction i.e. the current would slowly decrease with time at a given field. In the formed sample this effect is absent because, as mentioned above, the labile charged centers have been swept away and got fixed in a narrow region near the Al electrode.

Cadmium telluride

I-V measurements as well as measurements on photo-conductivity and photovoltage undoubtedly show that CdTe in these sandwiches appears as p-type material. Thus one could expect that switching would take place under conditions just opposite to those in CdSe which is actually not so. The very fact that the sandwiches of both p- and n-type materials reversibly switch in a cycle from low to high conductivity ohmic state on the application of negative voltage on Al electrode and vice versa, shows that the barrier operative in switching is not governed by the 'p' or 'n' character of the semiconductor but is due to an additional layer.

In order to arrive to such a model let us start again from the high conductivity ohmic state. Band diagram of this state is given in the Fig. 3.30 (c). To switch to low conductivity state (barrier present) one has to make Al electrode positive. Instantaneously holes as majority carriers overflow to Au electrode while electrons as minority carriers flow to Al electrode where they get trapped in the very layer between the Al metal and the semiconductor, rising the energy band diagram in that region as is shown in Fig. 3.30 (d) and a barrier is formed. On the other hand, viewed from semiconductor side the other barrier is also

formed due to the ionized acceptors which cause band to bend downwards. As a result we have now two barriers near Al electrode which oppose each other. Having this model in mind it is easy to imagine that the I-V dark characteristic of such a sandwich will give high dark resistance for both directions since one of the barriers will be always reverse biased. The resultant I-V behaviour will depend only of the reverse biased characteristic of one of the two available barriers.

On this basis it is easily understood why in our experimental work we could distinguish two extreme types of the I-V characteristics in CdTe sandwiches i.e. (i) good rectifying and (ii) non-rectifying as well as various intermediates between these two. Which characteristic will predominate is determined by the ability of the interfacial layer between the Al electrode and semiconductor to trap electrons. If this ability is large or if these electrons are bound firmly, a good barrier is formed which opposes the other barrier caused due to ionised acceptors. Thus, sandwich will remain blocking for both directions. If this is not so the sample be more rectifying i.e. it would give a higher forward current when Al electrode is made negative. Such a sample will never switch since a sufficient field is not developed.

On the basis of the proposed model it is not difficult to explain the unusual photovoltage performance (see Fig. 3.20), since there are two barriers (two photocells) which oppose each other.

The cell A has its origin in the barrier region on the semiconductor side. The electron-hole pair generated in this region is separated by the barrier and the electrons move to the left side of the barrier whereas the holes are collected on the gold electrode. This gives the gold electrode positive polarity with respect to aluminium electrode as is required by the experimental results.

The cell B has its origin in the barrier region on the side of the Al electrode. The electron-hole pair generated in this region is separated in the reverse way because of the reverse gradient. This gives the Al electrode positive polarity, which opposes the photovoltage of the cell A. If it is assumed that the magnitude of this voltage is greater than that of the cell A, then we can explain the voltage reversal.

Photoconductivity measurements are also easily explained. If Au is biased negatively, the photogenerated electrons will flow towards Al electrode (positive) and would collect in the large energy well between the two barriers.

This would make the barrier lower for hole injection from Al to the semiconductor and enhanced conductivity would be observed. On changing the polarity (Al electrode negative) electrons again will collect in the well because of the special energy gradient and would again decrease the barrier, now for the hole current from the semiconductor to aluminium electrode. Thus there would be enhanced conductivity for either direction of applied field as has actually been found experimentally.

The mechanism of switching has been discussed in great detailes for CdSe. The same mechanism seems to apply for CdTe as well, but one difference may be worth noting. Here we have two double layers in opposition i.e. as one moves from Al electrode towards the CdTe semiconductor, one meets first a negative charged layer followed by a positive layer and finally a negative space charge region. It is needless to say that in view of the electrical neutrality the total negative charge in the two regions must be equal to the positive charge in the central region. The migration of these charges leading to a complete collapse or thinning of the barrier, seems to be responsible for switching to the conducting state. On application of negative voltage on the Al electrode, the positive charged centres move towards the Al electrode. The negative space charge is also dragged

in the same direction in view of the attraction between these two regions. Thus the applied field concentrates the double layer in a very narrow region leading to a discharge of the double layer and loss of the barrier. Alternatively, the concentration of the space charge in a narrow region makes the barrier so thin that tunneling across this becomes possible and the barrier is no longer operative.

The time dependence of the dark current in case of CdTe can also be explained as in the case of CdSe. The only point to bear in mind that here one of the barrier is always reverse biased for any direction of the applied field. We should therefore expect only positive creep as has actually been observed. On the other hand in cases of extremely rectifying type samples, both positive and negative creep has been observed as expected i.e. rise of current with time under reverse bias and decay of current in forward bias.

These analyses do establish the existence of a single barrier in the case of CdSe and double barrier in the case of CdTe. This is also established that the switching, photoconductivity and relaxation phenomena are connected with these barriers and the associated ionic

processes. There could be some ambiguity about the exact way in which this barrier is removed or formed during switching but the models presented do appear to be most reasonable. Further experiments on capacitance measurement and spectral response measurements would no doubt throw more light on this and these experiments would be undertaken as soon as facilities become available.

. . . . .

SUMMARY

This thesis deals with some experimental investigations on aluminium-cadmium selenide, or telluride-gold sandwiches. The samples were prepared by sequentially depositing thin films of aluminium, CdSe or CdTe (purity 99.999 per cent) and gold on glass microscope slides. The CdSe or CdTe film was deposited from a silica boat heated by a tungsten wire in a vacuum of the order of 10^{-5} Torr. The thickness of the sample was 0.5 - 1.0 micron. The experimental arrangement was such that after each successive deposition, air had to be let in to make suitable adjustments. All depositions of CdSe or CdTe were done on substrates heated to 200 - 230°C. Deposited layers were annealed at 300 to 350°C in vacuum for about half an hour and cooled, and then the counter electrode was deposited. The current-voltage (I-V) characteristic was studied by using a low-frequency function generator as a source and a Tektronix type 515 oscilloscope as a recorder.

These sandwiches show interesting bistable conductivity, switching and memory phenomena. Initially, the virgin samples (preformation stage) show a rectifier-like current-voltage characteristic. After an initial

formation (post formation stage) they show bistable conductivity and cyclic switching between a high conductivity and low conductivity state which takes place continuously under applied cyclic voltage.

In the preformation stage all the CdSe sandwiches exhibit an asymmetric, rectifier-like I-V characteristics. However, the I-V characteristics of Al-CdTe-Au sandwiches are rather sensitive to preparation conditions. We could distinguish two types of samples, one which shows non-linear but only slightly asymmetric I-V characteristic and has a large resistance of the order of 10^5 ohms in both directions. For the other type there is a pronounced rectification observed.

Al-CdSe-Au sandwiches are forward biased by making Au electrode negative, which is contrary to what one would expect on the basis of the work function theory since CdSe is usually n-type material and Au has a higher work function. The structure is highly photosensitive, mainly when it is reverse-biased. Photocurrent increases rapidly with increasing applied reverse voltage.

In Al-CdTe-Au systems, the sandwiches which show rectification have the properties very similar to the Al-CdSe-Au samples discussed above. However, contrary

to CdSe, the telluride sandwich is forward biased when Au electrode is made positive. Like CdSe, this sample is also photosensitive mainly when reverse-biased. In Al-CdTe-Au system, the sandwiches which do not show pronounced rectification, show a pronounced photoconductivity and this is observed for both directions of applied voltage.

If one applies a negative voltage on Al electrode of a value greater than a critical voltage (V_A), the sample switches from low conductivity state to a highly conducting ohmic state. It remains in this state as long as a certain critical voltage (V_c) of reverse polarity (i.e.Al+) is not exceeded. On exceeding this critical voltage the sample switches back to the low conductivity state.

On making Al negative again and exceeding the threshold voltage V_A the sample switches back to the conducting state. The sample will switch from low to high conductivity state, and vice versa in a cycle under a cyclic voltage of a small repitition frequency. It is generally possible to establish switching only if one can apply a sufficiently high negative voltage on the Al electrode without passing an excessive current.

It is thus seen that in the post formation state the sample can exist in either of the two states :

(i) low conductivity state or (ii) high conductivity state. The state (i) is attained after a positive voltage greater than V_C has been applied to the aluminium electrode and remains stable so long as the negative voltage V_A is not exceeded. It can be cycled any number of times reversibly between the voltage V_A on the negative side and a corresponding voltage on the positive side. The state (ii) is attained after a negative voltage of magnitude greater than V_A has been applied and remains stable so long as the positive voltage V_C is not exceeded.

The samples show strong relaxation effects in the preformation stage. There are two types of relaxation : (i) slow rise of current with time found in samples under reverse bias and (ii) the instantaneous rise followed by a slow decay when the sample is forward biased. The later appears mainly in CdSe sandwiches which always show very pronounced rectification having a low forward resistance. The samples also show photovoltaic and photoconducting effects in the preformation stage.

The observed experimental results on the current-voltage-temperature dependence and the photoeffects in the preformation stage leads us to conclude that (i) CdSe is n-type and CdTe p-type (ii) Au-semiconductor contact is

ohmic, whereas Al-semiconductor contact is blocking (iii) the blocking contact arises due to surface states as well as a barrier layer. The adsorbed oxygen appears to play an important role in the creation of the barrier layer and (iv) there are two barriers in opposition at Al-CdTe interface.

It is concluded that the switching from the high to low conductivity state and vice versa involves alternate creation and removal of the barrier present at the Al-semiconductor interface. It is visualised that when Al is made positive, a double layer with negative charge on the side of the Al electrode and positive charge on the side of semiconductor is created. This gives rise to the blocking barrier. On reversing the polarity, the oppositely charged layers move closer and the double layer either becomes quite narrow and transparent, or is completely neutralised leading to removal of the barrier.

. . . . .

REFERENCES

1. Tamm, I., Phys. Z. Sovietunion, 1, 733 (1932).
2. Shockley, W., Phys. Rev., 56, 317 (1939).
3. Bardeen, J., ibid., 71, 717 1947.
4. Henisch, H.K., Rectifying Semi-conductor contacts, Oxford at the Clarendon Press (1957.
5. Schottky, W., Z. f. Phys., 113, 367 (1939).
6. Mott, N. F., Proc. Roy. Soc., A 171, 27 & 114 (1939).
7. Bethe, H. A., Massachussetts Ins. of Tech. Radiation Labor. Report, 43/12. (1942).
8. Mott, N.F. and Gurney, R.W., Electronic Processes in Ionic Crystals, Oxford University Press, London, p. 168 (1940).
9. Rose, A., Phys. Rev., 97, 1538 (1955).
10. Smith, R. W., and Rose, A., ibid., 97, 1531 (1955).
11. Zuleeg, R and Muller, R.S., Solid State Electronics, 7, 575 (1964).
12. Dresner, J and Shallcross, F.V., ibid., 6, 193 (1963).
13. Lampert, M.A., RCA Rev., 20, 682 (1959).
14. Lampert, M.A., Phys. Rev., 125, 126 (1962).
15. Lampert, M.A. and Rose, A., ibid., 121, 26 (1961).
16. Parmenter, R.H. and Ruppel, W., J. Appl. Phys., 30, 1548 (1959).
17. Lampert, M.A., Proc. IRE., 50, 1781 (1962).
18. Frenkel, J., Phys. Rev., 36, 1604 (1930).
19. Sommerfield, A. and Bethe, H. Handbuch der Physic von Geiger and Scheel (Verlag Julius Springer, Berlin), Aufl. 24/2. p. 450 1933.

20. Holm, R. and Kirschestein, B., Z. Tech. Physik., 16, 488 (1935).

21. Holm, R., J. Appl. Phys., 22, 569 (1951).

22. Mead, C.A., Proc. IRE., 48, 359 (1960)

23. Fisher, I.C. and Giaver, I., J. Appl. Phys., 32, 172 (1961).

24. Penley, J.C., Phys. Rev., 128, 596 (1962).

25. Geppert, D.V., J. Appl. Phys., 33, 2933 (1962).

26. Pittelli, E., Solid State Electronics, 6, 667 (1963).

27. Franz, W., Ann. Physic., 11, 17 (1952).

28. Boer, K.W. and Kummel, H., Z. Naturf., 9A, 177 (1954).

29. Von Hippel, A., Z. f. Physic., 68, 309 (1931).

30. Von Hippel, A., ibid., 75, 145(1932).

31. Von Hippel, A., Phys. Rev., 54, 1096 (1938).

32. McKay, K.G. and McAfee, K.B., J. Appl. Phys., 34, 329 (1963).

33. Zener, C., Proc. Roy. Soc. (London), A145, 523 (1934).

34. Ryvkin, S.M., Photoelectric Effects in Semiconductors, Consultant Bureau, New York, 1964.

35. Rose, A., Procid. IRE., 43, 1850 (1955).

36. Bube, R.H., Photoconductivity of Solids, J. Wiley & Sons., Inc., 1960.

37. Gunn, J.B., Proc. Phys. Soc. (London), 69B, 781 (1956).

38. Chopra, K.L., Proc. IEEE, 51, 941 (1963).

39. Chopra, K.L., ibid., 51, 1242 (1963).

40. Chopra, K.L., J. Appl. Phys., 36, 184 (1965).

41. Geppert, D.V., Proc. IEEE, 51, 223 (1963).

42. Hening, H.P., Phys. Status Solidi, 26, 225 (1968).

43. Steel, M.C. et. al., J. Phys. Doc., Japan, 19, 1729 (1962).

44. Beam, W.R. and Armstrong, A.L., Proc. IEEE, 52, 300 (1964).

45. Ridley, B.K., Proc. Phys. Soc. (London), 82, 954 (1963).

46. Van Heck, H.F., Phys. Letters, 26A, 175 (1968).

47. Kromer, H., Phys. Rev., 109, 1856 (1958).

48. Ridley, B.K. and Watkins, T.B., Proc. Phys. Soc. (London), 78, 293 (1961).

49. Ridley, B.K. and Watkins, T.B., J. Phys. Chem. Solids, 22, 155 (1961).

50. Ridley, B.K. and Pratt, R.G., Phys. Letters, 4, 300 (1963).

51. Hickmott, T.W., J. Appl. Phys., 33, 2669 (1962).

52. Pollack, S.R., et.al., Electrochem. Technol., 1, 96, (1963).

53. Hickmott, T.W., J. Appl. Phys., 35, 2118 (1964).

54. Ephstein, E.M., Sov. Phys. Solid State, 8,224 (1966).

55. Ioffe, J.V., ibid., 8, 234 (1966).

56. Pemidenkov, A.A. et.al., Sov. Phys. JETP., 23, 84 (1966).

57. Bonch-Bruevich, U.L., Sov. Phys. Solid State, 8, 290 (1966).

58. Thanova, et.al., ibid., 8, 632 (1966).

59. Boer, K.W., Phys. Rev., 139A, 1959 (1965).

60. Mead, C.A. and Spitzer, W.G., Phys. Rev., Letts., 10, 471 (1963).

61. Mead, C.A. and Spitzer, W.G., Phys. Rev., 134A, 713 (1964).

62. McWhorter, A.L. and Rediker, R.H., Proc. IRE., 47, 1207 (1959).

63. Kessler, J.O. and Tompkins, B.E., Solid State Electronics, 6, 297 (1963).

64. Hiatt, W.R. and Hickmott, T.W., Appl. Phys. Letts., 6, 106 (1965).

65. Mizushima, Y. et al., Proc. IEEE, 53, 322 (1965).

66. Mizushima, Y. et al., ibid., 53, 509 (1965).

67. Takagi, T. and Mizushima, Y., Proc. IEEE, 55, 477 (1967).

68. Patil, S.G. and Sinha, A.P.B., Brit, J. Appl. Phys., 18, 361 (1967).

69. Sakamoto, H., J. Electrochem. Soc., 114, 725 (1967).

70. Simmons, J.G. and Verderber, R.R., Proc. Roy. Soc., A301, 1464 (1967).

71. Verderber, R.R., et. al., Phil. Mag. 16,1049 (1967).

72. Argall, F., Solid State Electronics, 11, 535 (1968)

73. Lampert, M.A., Phys. Rev., 103, 1648 (1956).

74. Feldman, C. and Gutierrez, W., J. Appl. Phys., 39, 2474 (1968).

75. Stafeev, V.I., Sov. Phys. Solid State, 1, 763 (1959).

76. Ovshinsky, S.R., Phys. Rev. Letts., 21, 1450 (1968).

77. Boer, K.W. et al., Phys. Status Solidi, 1, 231 (1961).

78. Dussell, G.A. and Bube, R.H., J. Appl. Phys., 37, 2797 (1966)

79. Antic, B.M. and Sinha, A.P.B., Proc. IEEE, 56, 1259 (1968).

80. Pauling, L., The nature of chemical bond, Cornell University Press, Ithaca, N.Y. 1960.

81. Baubinos, R. et al., Phys. Status Solidi, 24, K91-3 (1967).

82. Jenny, D.A. and Bube, R.H., Phys. Rev., 96, 1190 (1954)

83. Bube, R.H., J. Electrochem. Soc., 113, 793 (1966).

84. Bube, R.H., J. of Chem. Phys., 27, 496 (1957).

85. Sheer, H. et.al., J. Electrochem. Soc., 112, 1002 (1965).

86. Brodie, D.A. and LaCombe, J., Canada. J. Phys., 45, 1353 (1967).

87. De Nobel, D., Physica, 22, 252 (1956).

88. Shalimova, K.V. et.al., Soviet. Phys. Cryst., 11, 431 (1966).

89. Palatnik, L.S. and Sorokin, V.K., Soviet Phys. Solid State, 8, 2233 (1967).

90. Semiletov, S.A., ibid., 4, 909 (1962).

91. Semiletov, S.A., Soviet Phys. Cryst., 1, 236 (1956).

92. De Klerk, I. et al., Rev. Sci. Instr., 36, 506 (1965).

93. Matsuno, J. and Inoue, M., Japan J. Appl. Phys., 6, 297 (1967).

94. Novik, F.T., Soviet Phys. Solid State, 5, 2300 (1964).

95. Somarjai, G.A., J. Phys. Chem. Solids, 24, 175 (1963).

96. Shimizu, K., Japan. J. Appl. Phys., 4, 627 (1965).

97. Brodie, D.E. and Reed, L.D., Canad. J. Phys., 43, 689 (1965).

98. Pensak. L., Phys. Rev., 109, 601 (1958).

99. Goldstein, B., ibid., 109, 601 (1958).

100. Komaschenko, V.N. and Fedorus, G.A., Soviet Phys. Semicon., 1, 4 (1967).

101. Swank, R.K., Phys. Rev., 153, 844 (1967).

102. Geppert, D.V. et al., J.Appl. Phys., 37, 2458 (1966).

103. Mead, C.A., Solid State Electronics, 9, 1023 (1966).

104. Cowley, A.M. and Sze, S.M., J. Appl. Phys., 36, 3212 (1965).

105. Spitzer, W.G. and Mead, C.A., ibid., 34, 3061 (1963).

106. Goodman, A.M., ibid., 34, 329 (1963).

107. Goodman, A.M., ibid., 35, 573 (1964).

108. Dore, B.V. et al., ibid., 37, 2458 (1966).

109. Learn, J.A. et al., Appl. Phys. Letts., 8, 144 (1966).

110. Terasaki, Y. et al., Elec. Commn. Labor., (Japan), 14, 425 (1966).

111. Adirovich, E.I. et al., Soviet. Phys. Solid State, 7, 759 (1965).

112. Smith, R.W., Phys. Rev., 97, 1525 (1955).

113. Zuleeg, R. and Muller, R.S., Solid State Electronics, 7, 575 (1964).

114. Nakai, J. et al., Japan J. Appl. Phys., 3, 490 (1963).

115. Bujati, M., British J. Appl. Phys. (D), Ser. 2, Vol. 1, 581 (1958).

116. Schottky, W., Z. f. Physic, 118, 539 (1942).

117. Emtage, P.R. and Tantraporn, W., Phys. Rev. Letts., 8, 267 (1962).

118. Pollack, S.R., J. Appl. Phys., 34, 877 (1963).

119. Johnson, V.A. et al., ibid., 21, 283 (1950).

120. Mumata, T., Mem. Fac. Sci. Kyusyu University B, 1, 79 (1953).

121. Henisch, H.K. and Ewels, J., Proc. Phys. Soc., B63, 861 (1950).

122. Cooper, R. and Harrington, J., ibid., B65, 303 (1952).

123. Hayashi, T., Japan. J. Appl. Phys., 3, 230 (1964).

124. Gershun, A.S. et al., Soviet Phys. Solid State, 8, 2495 (1967).

125. Gershun, A.S. et al., Soviet Phys. Solid State, 8, 2982 (1967).

126. Snow, E.H. et al., J. Appl. Phys., 36, 1664, (1965).

127. Williams, R. and Bube, R.H., ibid., 31, 968 (1960).

128. Chopra, K.L., Solid State Electronics, 8, 715 (1965).

129. Gibson, A.F., Proc. Phys. Soc., 65B, 196 (1952).

130. Petritz, R.L., Phys. Rev., 104, 1058 (1956).

. . . . .